SABRE-LL-I

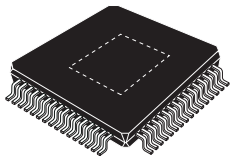
Combo motor driver

Preliminary Data

Features

- Configurable device
- 4 full bridges to generate
  - Up 2 DC motor drivers and 1 stepper motor driver

  or
  - 4 DC motor drivers
- Bridges (1 & 2) additional configurations are
  - Super DC
  - 2 half bridges
  - 1 super half bridge
  - 2 switches
  - 1 super switch
- Bridges (3 & 4) additional configurations are:
  - Same as bridges 1&2, listed above
  - 2 buck regulators (bridge 3)
  - 1 super buck regulator
  - Battery charger (bridge 4)
- One variable voltage buck switching regulator
- One switching regulator controller
- One linear regulator
- Bidirectional serial interface
- Programmable watchdog function
- Integrated power sequencing and supervisory functions with fault signaling through serial interface and external reset pin
- Thermal shutdown protection with thermal warning capability
- Very low power dissipation in shut-down mode (~35 mW)



TQFP64 exposed pad

- Aux features
  - Operational amplifiers
  - Comparators
  - Pass switches
  - Multi-channels 9 bit ADC
  - GPIOs

Description

S.A.B.Re™ (structured architecture of bridges and regulators) is a new concept of IC in the motion & power supply field. ST aim is to follow the S.A.B.Re specification and to offer to the customer an IC with a wide number of features, that can be configured and customized: motor drivers, regulators, high precision A/D converter, operational amplifiers and voltage comparators.

The start up configuration can be defined by the GPIOs and then through the serial interface; a customization can be done through a metal layer in order to set more complex functions.

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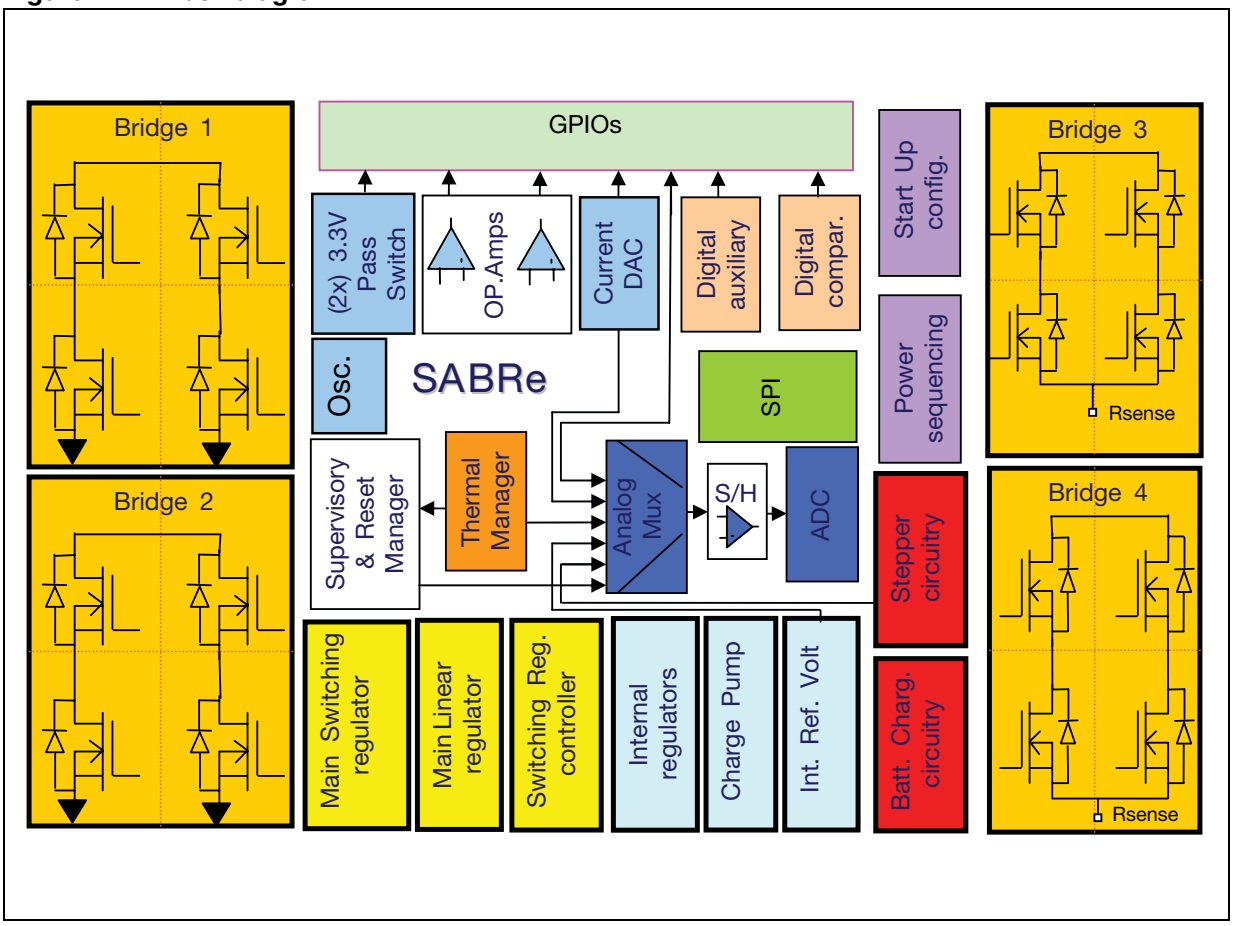
1 General description

1.1 Overview

S.A.B.Re represents a new concept of IC in motion & power supply field.

The aim that ST followed in defining S.A.B.Re specification was to offer to the customer an IC with a wide number of features: motor drivers, regulators, high precision A/D converter, operational amplifiers, voltage comparators and many other circuits can easily be configured and customized. The device configuration can be defined by programming the IC via the Serial Interface while a deeper customization can be done through metal layer in order to set more complex functions.

Figure 1. Block diagram



Note: See following "S.A.B.Re's Main features" for a detailed description of possible configurations.

2 S.A.B.Re's main features

S.A.B.Re includes the following circuits:

- Four widely configurable full bridges:
  - Bridges 1 and 2:
    - Diagonal RDSon: 0.6Ω typ.
    - Max operative current = 2.5A.
  - Bridges 3 and 4:
    - Diagonal RDSon: 0.85Ω typ.
    - Max operative current = 1.5A.
- Possible configurations for each bridge are the following:
  - Bridge 1:
    - DC motor driver.
    - Super DC (bridge 1 and 2 paralleled form superbridge1).
    - 2 independent half bridges.
    - 1 super half bridge (bridge 1 side A and bridge 1 side B paralleled form superhalfbridge1).
    - 2 independent switches (high or low side).
    - 1 super switch (high or low side).
  - Bridge 2 has the same configurations of bridge 1.
  - Bridge 3 has the same configurations of bridge 1 (bridge 3 and 4 paralleled form superbridge2) plus the following:
    - ½ Stepper motor driver.
    - 2 buck regulators (V_{AUX1_SW}, V_{AUX2_SW}).
    - 1 Super buck regulator ($V_{AUX1//2\_SW}$).
  - Bridge 4 has the same configurations of bridge 1 plus the following:
    - ½ stepper motor driver.
    - 1 super buck regulator (V_{AUX3_SW}).
    - Battery charger.
- One buck type switching regulator (V_{MAIN_SW}) with:
  - Output regulated voltage range: 1-5 Volts.
  - Output load current: 3.0 A.
  - Internal output power DMOS.
  - Internal soft start sequence.
  - Internal PWM generation.
  - Switching frequency: ~250kHz.
  - Pulse skipping strategy control.
- One switching regulator controller (V_{EXT_SW}) with:
  - Output regulated voltage range: 1-30 Volts.
  - Selectable current limitation.
  - Internal PWM generation.
  - Pulse skipping strategy control.

- One linear regulator (V_{MAIN_LIN}) that can be used to generate low current/low ripple voltages. This regulator can be used to drive an external bipolar pass transistor to generate high current/low ripple output voltages.
- One bidirectional serial interface with address detection so that different ICs can share the same data bus.
- Integrated power sequencing and supervisory functions with fault signaling through serial interface and external reset pin.
- Fourteen general purpose I/Os that can be used to drive/read internal/external analog/logic signals.
- One 8-bit/9-bit A/D converter (100KS/sec @ 9-bit, 200KS/sec @8-bit). It can be used to measure most of the internal signals, of the input pins and a voltage proportional to IC temperature.
  - Current sink DAC:
  - Three output current ranges: up to 0.64/6.4/64 mA.
  - 64 (6-bit programmable) available current levels for each range.
  - 5V output tolerant.
- Two operational amplifiers:
  - 3.3V supply, rail to rail input compatibility, internally compensated.
  - They can have all pins externally accessible or can be internally configured as a buffer o make internal reference voltages available outside of the chip.
  - Unity gain bandwidth > 1MHz.
  - They can also be set as comparators with 3.3V input compatibility and low offset.
- Two 3.3V pass switches with 1Ω RDSon and short circuit protected.
- Programmable watchdog function.
- Thermal shutdown protection with thermal warning capability.
- Very low power dissipation in "Low Power mode" (~35mW)
- S.A.B.Re is intended to maximize the use of its components, so when an internal circuit is not used it could be employed for other applications. Bridge 3, for example, can be used as a full bridge or to implement two switching regulators with synchronous rectification: to obtain this flexibility S.A.B.Re includes 2 separate regulation loops for these regulators; when the bridge is used as a motor driver, the 2 regulation loops can be redirected on general purpose I/Os to leave the possibility to assembly a switching regulator by only adding an external FET.

3 Global specifications

3.1 Absolute maximum rating specifications

The following specifications define the maximum range of voltages or currents for S.A.B.Re.

Stresses above these absolute maximum specifications may cause permanent damage to the device.

Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 2. Absolute maximum rating

Parameter	Description	Test condition	Min	Max	Unit
V_{Supply_Abs}	V_{Supply} voltage			40	V
$V_{GPIO\_SPI\_Abs}$	V_{GPIO_SPI} voltage			3.9	V
V_{3V3pin_Abs}	3.3V pins input voltage			3.9	V
V_{Sw_Abs}	Switching regulators output pin voltage range		-1	V_{Supply}	V
V_{Sw_pulse}	Switching regulators min pulsed voltage	For less than 500ns	-3		V
V_{Pump_Abs}	Charge pump pins voltage	(1)		15	V
T_{j_Abs}	Junction temperature(2)	Storage	-40	190	°C
		Operating	0	TSD	°C

1. This value is useful to define the voltage rating for external capacitor to be connected from V_{Pump} to V_{Supply}. V_{Pump} is internally generated and can never be supplied by external voltage source nor is intended to provide voltage to external loads.
2. TSD is the thermal shut down temperature of the device.

3.2 Operating ratings specifications

Table 3. IC operating ratings

Parameter	Description	Test condition	Min	Max	Unit
V_{Supply_Op}	V_{Supply} voltage range		23	38	V
I_{Supply_Op}	V_{Supply} operative current	(1)		15	mA
I_{Shut_down}	V_{Supply} shut down state current			1.5	mA
$V_{GPIO\_SPI\_OP}$	V_{GPIO_SPI} voltage range		2.4	3.6	V
$I_{VGPIO\_SPI\_OP}$	V_{GPIO_SPI} operative current	(2)		TBD	mA
V_{3v3pin_Op}	3.3V input pins voltage range		-0.3	3.6	V
T_{j_Abs}	Junction temperature	Operating	0	125.	°C

1. Operating Supply current is measured with System regulators operating but not loaded.
2. Operating V_{GPIO_SPI} current is measured with all circuits supplied by V_{GPIO_SPI} (GPIO's, operational amplifiers and pass switches) enabled but not loaded.

4 Internal supplies

4.1 Overview

S.A.B.Re includes three internal regulators used to provide a regulated voltage to internal circuits.

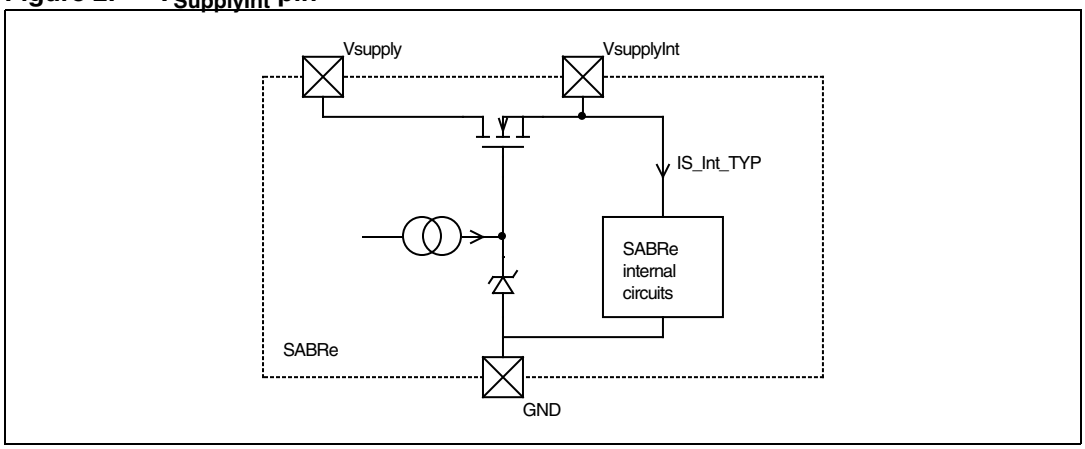
The internal regulators are the following:

- $V_{SupplyInt}$ regulator.
- Charge pump regulator.
- V_{3v3} regulator.

4.2 $V_{SupplyInt}$ regulator

$V_{SupplyInt}$ is the output of an internal regulator used to supply some internal circuits. This regulator is not intended to provide external current so it must not be used to supply external loads. An external capacitor must always be connected to this pin (preferably towards V_{Supply} pin).

Figure 2. $V_{SupplyInt}$ pin



The $V_{SupplyInt}$ pin may also be externally connected to V_{Supply} pin by means of an external resistor R_{EXT}: this allows R_{EXT}, particularly when V_{Supply} is at the max values of the operative supply range, to dissipate power that otherwise would be dissipated inside the chip. The choice of the optimal resistor depends on the application since it is strictly depending on both V_{Supply} and the current used inside the chip (that is changing with the chosen configuration).

4.3 $V_{SupplyInt}$ specifications

Table 4. $V_{SupplyInt}$ specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
$V_{S\_Int\_RNG}$	$V_{SupplyInt}$ output voltage	(1)	18	19.5	21	V
$I_{S\_Int\_TYP}$	$V_{SupplyInt}$ operative current	(2)		11		mA
R_{Ext}	External resistor value	V_{Supply}=32V I_{S_Int}=12mA(3)		1000	1.5	Ω
C_{Ext}	External capacitor		80	100	120	nF

1. This value is useful to define the voltage rating for external capacitor to be connected from V_{Supply} to $V_{SupplyInt}$.
2. This typical value is only intended to give an extimation of the current consumption when S.A.B.Re is configured in simple regulators mode (see following *Chapter 8.7.4*) at the end of the start up sequence and with no load on regulators. This typical value allows a raw choose of the external resistor but the definitive choose must be done according to following Note 3).
3. REXT could be chosen by applying this formula: REXT = ($V_{Supply\ min}$ - VS_Int max)/(I_{S_Int} max). I_{S_Int} max is depending from the chosen configuration and represents the total current needed by the circuits connected to this pin.

4.4 Charge pump regulator

S.A.B.Re implements a charge pump regulator to generate a voltage over V_{Supply}.This voltage is used to drive internal circuits and the external FET driver and cannot be used for any other purpose.

This circuit is always under the supervisory circuit control, so no regulator can start before the V_{Pump} voltage reaches its undervoltage rising threshold. If V_{Pump} voltage falls down below its under voltage falling threshold, all the regulators will be switched off.

The charge pump circuit is disabled when S.A.B.Re is in “Low Power mode”.

Table 5. V_{Pump} specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{Pump}	Regulated Voltage	V_{Supply}=32V	V_{Supply} +10.5	V_{Supply} +12.5	V_{Supply} +14.5	V
F_{Pump}	V_{Pump} clock frequency	Fosc = 16MHz typ		Fosc/64		KHz
C_{FLY}	Flying capacitor			100		nF
C_{BOOST}	Boost capacitor			1		µF

4.5 V3v3 regulator

V3v3 is the output of an internal regulator used to supply some low voltage internal circuits. This regulator is not intended to provide external current so it must not be used to supply external loads. An external capacitor must always be connected from this pin to gnd.

4.6 V3v3 specifications

Table 6. $V_{SupplyInt}$ specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{3V3}	V_{3v3} output voltage	V_{Supply}=32V	3.15	3.3	3.45	V
C_{Ext}	External capacitor		80	100	120	nF

5 Supervisory system

5.1 Overview

The supervisory circuitry monitors the state of several functions inside S.A.B.Re and resets the device (and other ICs if connected to nRESET pin) when the monitored functions are outside their normal range. Supervisory circuitry can be divided into three main blocks:

- Power on reset (POR) generation circuitry.
- nRESET (nRST_int) generation circuitry.
- Thermal shut down (TSD) generation circuitry.

POR circuitry monitors the voltages that S.A.B.Re needs to guarantee its own functionality; nRESET circuitry controls if S.A.B.Re's main voltages are inside their normal range; TSD is the thermal shut down of the chip in case of overheating.

5.2 Power on reset (POR) circuit

Power on reset circuit monitors V_{Supply}, and V3v3 voltages. The purpose of this circuit is to set the device is in a stable and controlled status until the minimum supply voltages that guarantee the device functionality are reached. The output signal of this circuit (in the following indicated as "POR") becomes active when V_{Supply} or V3v3 go under their falling threshold.

When POR output signal is active, all functions and all flags inside S.A.B.Re are set in their reset state; once POR signal comes back from off state (meaning monitored voltages are above their rising threshold), the power up sequence is re-initialized

Table 7. Power on reset specifications

Parameter	Description	Test condition	Min	Typ	Max	Unit
$V_{Supply\_POR\_valid}$	V_{Supply} voltage for POR valid	I_{nRESET} = 1mA	4			V
$V_{Supply\_POR\_fall}$	V_{Supply} POR falling threshold	V_{Supply} falling	6		9	V
$t_{Supply\_POR\_filt}$	V_{Supply} POR filter Time			3		µs
$V_{3V3\_POR\_fall}$	V_{3v3} POR falling threshold	V_{3V3} falling	1.9	2.2		V
$V_{3V3\_POR\_rise}$	V_{3v3} POR rising threshold	V_{3V3} rising		2.7		V
$V_{3V3\_POR\_hys}$	V_{3v3} POR hysteresis			0.5		V
$t_{3V3\_POR\_filt}$	V_{3v3} PORfilter time			1.5		µs

5.3 nRESET generation circuit

The nRESET circuit monitors V_{Supply}, V_{Supply_int}, V_{Pump}, V_{GPIO_SPI} and all system regulators (VSystem) voltages. The purpose of this circuit is to prevent the device functionality until the monitored voltages reach their operative value (please note that V_{3v3}

is monitored by POR, so it must be above its minimum value, otherwise nRESET circuit is not active).

This circuit generates an internal reset signal (in the following indicated as “nRST_int”) that will also be signaled to external circuits by pulling low the nRESET pin.

The signal nRST_int becomes active in the following cases:

1. When one of the following voltages is lower than its own under voltage threshold:
   - V_{Supply} and V_{Supply_int}.
   - V_{Pump}.
   - V_{System} (all switching or linear system regulators voltages).
   - V_{GPIO_SPI}.
2. When watchdog timer counter (see *Chapter 6*) elapse the watchdog timeout time (only if watchdog function is enabled).
3. When S.A.B.Re is in “Low Power mode”.
4. When EnExtSoftRst bit in SoftResReg register is at logic level = “1” and a “SoftRes” command is applied (see SoftResReg register description in *Chapter 25*).

When an nRST_int event is caused by above cases, the nRESET pin will stay low for a “stretch” time that starts from the moment that nRST_int signal returns in the operative state. This stretch time can be selected by setting the ID[1:0] bits in the SampleID register according to following table:

Table 8. Stretch time selection

ID[1]	ID[0]	Selected stretch time	Note
		Typ	
0	0	16ms	Default state
0	1	32ms	
1	0	48ms	
1	1	64ms	

When nRST_int becomes active (logic level = “0”) it sets in their reset state some of the functions inside S.A.B.Re. The main functions that will be reset by nRST_int signal are the following:

- Serial interface will be reset and will not accept any other command.
- The bridges 1 and 2 will place their outputs in high impedance and PWM and direction signals will be reset.
- Not system regulators will be powered off.
- AD converter will be powered off.
- GPIOs will be powered off.
- Current DAC will be powered off.
- Operational amplifiers will be powered off.
- Watchdog count will be reset (while Watchdog flags won’t be reset).
- Interrupt controller will be powered off.
- Digital comparator will be powered off.

Additionally the system regulators will be powered off but only if the voltage that caused the nRST_int event is checked before the system regulator in the power up sequence. This means that:

- all system regulators will be powered off if nRST_int is caused by V_{Supply}, V_{Supply_int}, V_{Pump} (and also if V3v3 causes a POR);
- no one of the system regulators will be powered off if nRST_int is caused by V_{GPIO_SPI};
- only the system regulators that follows the system regulator that caused the nRST_int in power up sequence will be powered off.

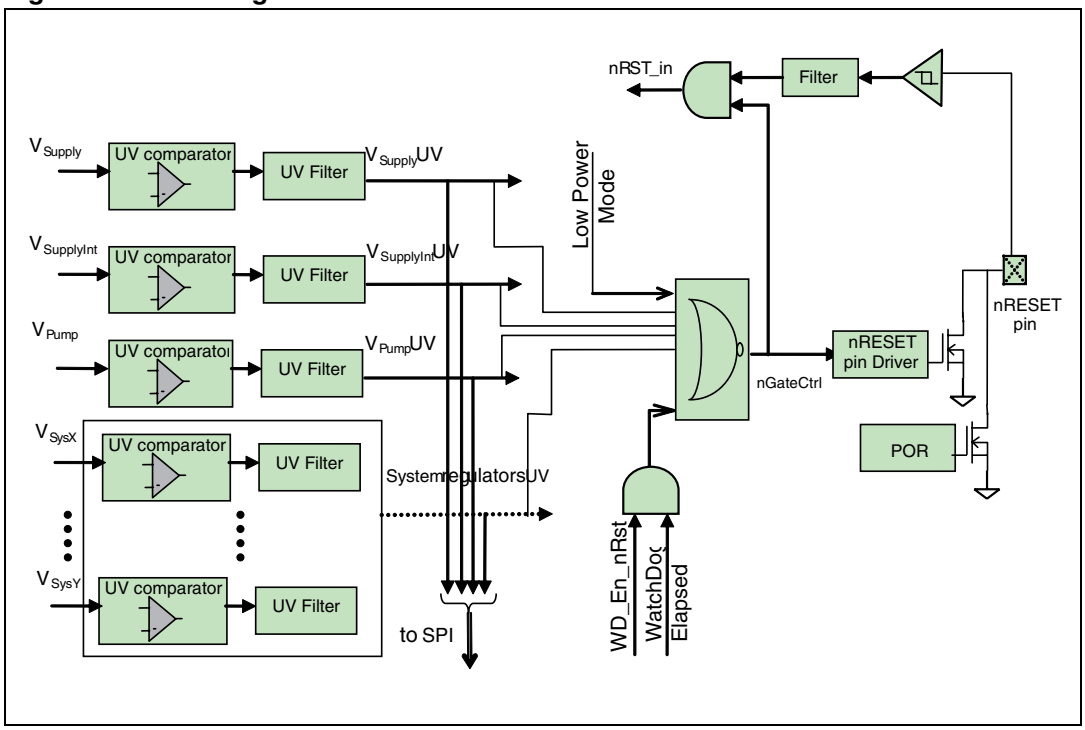
5.4 nRESET specifications

Table 9. nRESET circuit specifications

Parameter	Description	Test condition	Min	Typ	Max	Unit
nRST_VOL	nRESET Low level output voltage	I=10mA			0.4	V
nRST_fall	nRESET fall time	I=1mA C=50pF(1)			15	ns
nRST_del	nRESET delay time	(2)			150	ns
$V_{Supply\_UV\_f}$	V_{Supply} falling threshold		18.5			V
$V_{Supply\_UV\_r}$	V_{Supply} rising threshold				23	V
$V_{Supply\_UV\_hys}$	V_{Supply} hysteresis			2		V
t_{Supply_UV}	V_{Supply} UV filter time			3.5		us
$V_{S\_Int\_UV\_f}$	$V_{SupplyInt}$ falling threshold		14.0			V
$V_{S\_Int\_UV\_r}$	$V_{SupplyInt}$ rising threshold				17.5	V
$V_{S\_Int\_UV\_hys}$	$V_{SupplyInt}$ hysteresis			1.5		V
$t_{S\_Int\_UV}$	$V_{SupplyInt}$ UV filter time			3.5		µs
$V_{Pump\_UV\_f}$	V_{Pump} falling threshold		V_{Supply} +7			V
$V_{Pump\_UV\_r}$	V_{Pump} rising threshold				V_{Supply} + 9.5	V
$V_{Pump\_UV\_hys}$	V_{Pump} hysteresis			1.5		V
t_{Pump_UV}	V_{Pump} UV filter time			3.5		us
$V_{GPIO\_SPI\_UV\_f}$	V_{GPIO_SPI} falling threshold		1.8			V
$V_{GPIO\_SPI\_UVr}$	V_{GPIO_SPI} rising threshold				2.4	V
$V_{GPIO\_SPI\_hys}$	V_{GPIO_SPI} hysteresis			250		mV
$t_{GPIO\_SPI\_UV}$	V_{GPIO_SPI} UV filter time			3.5		us

1. Measured between 10% and 90% of output voltage transition.
2. Measured from a fault detection to 50% of output voltage transition.

Figure 3. nReset generation circuit



Note: All regulator voltages included in power up sequence (V_{SysX} – V_{SysY} in Figure 3) will be considered as nRESET circuit voltages.

5.5 Thermal shut down generation circuit

The third component of the supervisory circuit is the thermal shut down generation circuit.

This circuit generates two different flags depending on the IC temperature:

- the “TSD” flag indicates that the IC temperature is greater than the maximum allowable temperature.
- the “Warm” flag, that can be read using serial interface, becomes active at a lower temperature respect to TSD signal, therefore it can be used to prevent the IC from reaching over temperature.

When a TSD event occurs, S.A.B.Re will enter in the reset state placing the bridges in high impedance and turning off all regulators and other circuits until the internal temperature decreases below the Warm temperature. At this point, S.A.B.Re will restart the power up sequence and TSD bit will be set and will be readable as soon as S.A.B.Re will come out from the reset state.

This TSD bit can be reset in three ways:

- by writing a logic level ‘1’ in the ClearTSD bit in the ICTemp register (see *Chapter 25*);
- by a POR event;
- by entering in “Low Power Mode”.

The Warm bit, set by S.A.B.Re when IC is working over the warming temperature, can be read using the SPI interface. Once this bit is set it can be reset in three ways:

- by writing a logic level ‘1’ in the ClearWarm bit;
- by a POR event;
- by entering in “Low Power Mode”.

The thermal sensor voltage can be converted using the internal A/D: this way the microcontroller can directly measure the IC temperature.

To avoid unwanted commutation especially when temperature is near the thresholds, the output signal is filtered for both TSD and Warm.

5.6 TSD specifications

Table 10. TSD circuit specifications

Parameter	Description	Test condition	Min	Typ	Max	Unit
T_{TSD}	Thermal shut down temperature			170		°C
T_{WARM}	Warming temperature			140		°C
T_{DIFF}	Thermal shut down to warming difference			30		°C
t_{TSD_FILT}	Thermal shut down filter time			8		us
t_{WARM_FILT}	Warming filter time			8		us

6 Watchdog circuit

6.1 Overview

The Watchdog timer can be used to reset S.A.B.Re if it is not serviced by the firmware that can periodically write at logic level “1’ the ClrWDog bit in the WatchDogStatus register.

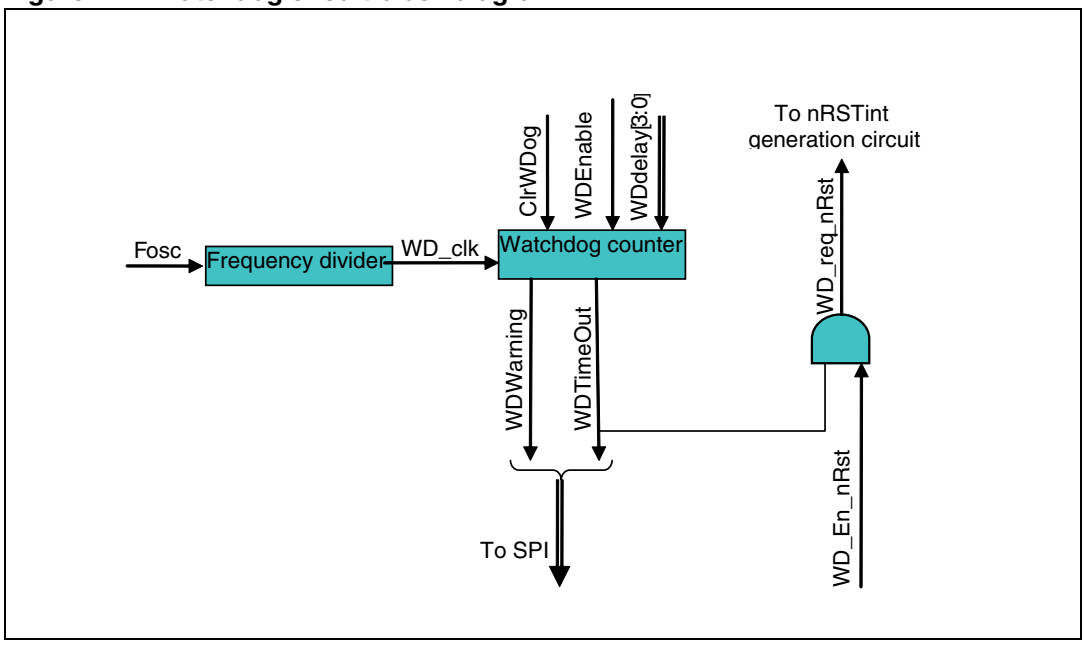
This circuit is disabled by default; firmware can enable it by setting at logic level ‘1’ the WDEnable bit in the WatchDogCfg register.

When the Watchdog timeout event happens, S.A.B.Re sets to ‘1’ a latched bit WDTimeOut in theWatchDogStatus register that can be read using SPI interface; once this bit is set it can be cleared in three ways:

- by writing a ‘1’ in the WDClear bit in the WatchDogStatus register.
- by writing a ‘1’ in the SoftReset bit in the WatchDogStatus register.
- by a POR event.

The Watchdog function includes also a warning bit WDWarning to indicate, via serial interface or via the circuit called Interrupt Controller (see *Chapter 21*) that the watchdog is near to its timeout; this bit is asserted to logic level “1” exactly one watch dog clock period (WD_Tclk) before the watchdog timeout happens. Firmware can enable the WDTimeOut signal to cause an “nRst_int” event by setting to logic ‘1’ the WDEnnRst bit.

Figure 4. Watchdog circuit block diagram



The watchdog timeout has an imprecision of maximum one WD_Tclk. The effective programmed WD time is changed in the register only when the watchdog circuit is serviced by firmware with ClrWDog bit. At this time the watchdog timer is reset and the new value of the WD delay value is loaded.

The watchdog timer can be programmed to generate different timeouts using the WDdelay[3:0] bits in the WatchDogCfg register according to following table:

Table 11. Watchdog timeout specifications

WDdelay[3:0]	WD timeout
	Typ
0000	8*WD_Tclk
0001	9*WD_Tclk
0010	10*WD_Tclk
0011	11*WD_Tclk
0100	12*WD_Tclk
0101	13*WD_Tclk
0110	14*WD_Tclk
0111	15*WD_Tclk
1000	16*WD_Tclk
1001	17*WD_Tclk
1010	18*WD_Tclk
1011	19*WD_Tclk
1100	20*WD_Tclk
1101	21*WD_Tclk
1110	22*WD_Tclk
1111	23*WD_Tclk

6.2 Watchdog specifications

Table 12. Watchdog specifications

Parameter	Description	Test condition	Min	Typ	Max	Unit
WD_Tclk	Watchdog clock period			Tosc * 2^{22}		s

7 Internal clock oscillator

7.1 Overview

S.A.B.Re includes a free running oscillator that does not require any external components.

This circuit is used to generate the time base needed to generate the internal timings; the typical frequency is 16MHz.

The oscillator circuit starts as soon as the IC exits from the power on reset condition and it is stopped only when in “Low Power mode”.

7.2 Internal clock specifications

Table 13. Internal clock specifications

Parameter	Description	Test condition	Min	Typ	Max	Unit
F_{osc}	Oscillator frequency	V_{3V3} =3.3V	14.4	16	17.6	MHz
T_{osc}	Oscillator period		1/Fosc			

8 Start-up configurations

8.1 Overview

S.A.B.Re start-up configuration is selected by setting in different states the GPIO[0], GPIO[3] and GPIO[4] pins. Each of these is a three state input pin and is able to distinguish among the following situations:

Table 14. Possible start-up pins state symbol

Pin condition	State symbol
Shorted to ground	0
Shorted to V_{3v3} pin	1
Floating	Z

Note: “Shorted” means: R≤1KOhm; “Z” means: R≥10KOhm, C≤200pF

8.2 Operation modes

When V_{Supply} voltage is applied to S.A.B.Re, the internal regulator V3v3, used to supply the logic circuits inside the device, starts its functionality. When it reaches its final value, S.A.B.Re enables the GPIO[0] pin state read circuitry, and, after a time TpinSample, it will sample the GPIO[0] state. If it is found to be in high impedance, S.A.B.Re does not consider GPIO[3] and GPIO[4] pins state and starts its “Basic device” mode sequence. If GPIO[0] is found to be connected to ground or to V3v3, S.A.B.Re checks the state of GPIO[3] and GPIO[4] pins to select its start-up configuration.

The possible configurations can be classified in four “Major” modes:

1. Basic device.
2. Slave device.
3. Master device.
4. Single device.

Hereafter is reported the correspondence table between GPIO[X] state and S.A.B.Re configurations.

Table 15. Start-up correspondence

Pin state[1]			Major mode	Minor mode[2]
GPIO[0]	GPIO[3]	GPIO[4]		
Z	X	X	Basic	
0	0	0	Single	Bridge
0	0	Z		Primary regulator
0	0	1		Regulators
0	Z	0		Simple regulator
0	Z	Z		Bridge + VEXT
0	Z	1		Secondary Regulators
0	1	0	Master	Bridge
0	1	Z		Primary regulator
0	1	1		Regulators
1	0	0		Simple regulator
1	0	Z		Bridge + VEXT
1	0	1		Secondary Regulators
1	Z	0	Slave	Bridge
1	Z	Z		Primary regulator
1	Z	1		Regulators
1	1	0		Simple regulator
1	1	Z		Bridge + VEXT
1	1	1		Secondary Regulators.

1. “X” means “don’t care”.
2. The description of these modes is in the following paragraph 9.7.

8.3 Basic device mode

The basic device mode is selected by leaving the GPIO[0] pin floating. In this mode S.A.B.Re doesn’t use GPIO[3] and GPIO[4] as configuration pins, leaving them free for other uses.

When in this mode the regulators included in the start up sequence (except V_{MAIN_SW}) are considered as system regulators and they start in the following sequence:

1. Auxiliary switching regulator1 (V_{AUX1_SW}).
2. Auxiliary switching regulator2 (V_{AUX2_SW}).
3. Main linear regulator (V_{MAIN_LIN}).
4. Main switching regulator (V_{MAIN_SW}) (Not system regulator).

8.4 Slave device mode

In slave device mode, S.A.B.Re consider the nAWAKE pin as an input enable. Since this is now a digital pin, the current pull up source inside the nAWAKE circuit is disabled.

At the startup, if the nAWAKE pin is found to be low for a period higher than $t_{AWAKEFILT}$ seconds, S.A.B.Re enters directly in the “Low Power mode”; when nAWAKE pin is pulled high for a period higher than $t_{AWAKEFILT}$ seconds, S.A.B.Re begins its start up procedure.

8.5 Master device mode

In master device mode, S.A.B.Re begins its start up procedure without waiting for any external enable signal and it uses GPIO[5] pin to drive the nAWAKE pin of Slave devices.

During the whole start up time, it forces its GPIO[5] pin at logic level “0” in order to maintain all slave devices in “Low Power mode” as previously described. When start up operations are completed, S.A.B.Re forces the GPIO[5] output to logic level “1” to enable the slave devices and keeps GPIO[5] output at high level until it senses an under-voltage on any of its System regulators. If firmware writes in the PwrCtrl register to set Master S.A.B.Re in “Low Power mode” it immediately forces GPIO[5] output to logic level “0” to force the slave devices to enter in “Low Power mode”, then it waits for $T_{MASTWAIT}$ time and it starts its “Low Power mode” sequence.

8.6 Single device mode

In single device mode, the device behaves similarly to master device mode but:

1. It doesn’t use the GPIO[5] pin to drive slave devices.
2. It doesn’t wait for $T_{MASTWAIT}$ before entering in “Low Power mode”.

8.7 Sub-configurations for slave, master or single device modes

Each slave, master or single device modes can be divided in other minor modes depending on the start-up sequence needed for S.A.B.Re internal regulators.

Unless otherwise specified, in all the following modes the regulators included in the start up sequence are considered system regulators and they start in the sequence indicated.

8.7.1 Bridge mode

In this configuration bridges 3 and 4 are not used as regulators and therefore can be configured by the firmware in any of their possible bridge modes.

When in this mode the power-up sequence is:

1. Main switching regulator (V_{MAIN_SW}).
2. Main linear regulator (V_{MAIN_LIN}).

8.7.2 Primary regulator mode (KP)

In this configuration bridge 4 can be configured by firmware while bridge 3 is configured as two separate synchronous switching regulators. The last regulator in the sequence (V_{AUX2_SW}).is not considered a system regulator.

When in this mode the power-up sequence is:

1. Auxiliary switching regulator1 (V_{AUX1_SW}).
2. Main switching regulator (V_{MAIN_SW}) together with main linear regulator (V_{MAIN_LIN}).
3. Auxiliary switching regulator2 (V_{AUX2_SW}) (Not system regulator).

8.7.3 Regulators mode

In this configuration bridge 4 can be configured by firmware while bridge 3 is configured as two separate synchronous switching regulators, but the start up sequence is different previous one.

When in this mode the power-up sequence is:

1. Main switching regulator (V_{MAIN_SW}).
2. Auxiliary switching regulator1 (V_{AUX1_SW})
3. Auxiliary switching regulator2 (V_{AUX2_SW})

8.7.4 Simple regulator mode (KT)

Also in this configuration Bridge 4 can be configured by firmware while Bridge3 is configured as two separate synchronous switching regulators. The last regulator in the sequence (V_{MAIN_SW}).is not considered a system regulator.

When in this mode the power-up sequence is:

1. Auxiliary switching regulator1 (V_{AUX1_SW}).
2. Auxiliary switching regulator2 (V_{AUX2_SW})
3. Main linear regulator (V_{MAIN_LIN})
4. Main switching regulator (V_{MAIN_SW}) (not system regulator).

8.7.5 Bridge+ V_{EXT} mode

In this configuration bridges 3 and 4 are not used as regulators and the regulator obtained using the switching regulator controller (V_{EXT}) is included in start-up.

When in this mode the power-up sequence is:

1. Main switching regulator (V_{MAIN_SW}).
2. Switching regulator controller regulator (V_{EXT}).
3. Main linear regulator (V_{MAIN_LIN}).

8.7.6 Secondary regulators mode

In this configuration, bridge 3 is configured as a single synchronous switching regulator using its two half bridges in parallel ($V_{AUX\_(1//2)SW}$).

When in this mode the power-up sequence is:

1. Main switching regulator (V_{MAIN_SW}).
2. Auxiliary switching regulator ($V_{AUX(1//2)\_SW}$).
3. Main linear regulator (V_{MAIN_LIN}).

9 Power sequencing

9.1 Overview

As soon as V_{Supply} and $V_{SupplyInt}$ are above their power on reset level, S.A.B.Re will start the charge pump circuit; once V_{Pump} voltage reaches its under voltage rising threshold, S.A.B.Re begins a sequence that starts the regulators considered system regulators.

A regulator is considered a System regulator if:

- It has to start in on state without any user action.
- It is included in the power-up sequence.
- Its under-voltage event is considered by S.A.B.Re as an error condition to be signaled through nRESET pin.

Once V_{Supply} and $V_{SupplyInt}$, V_{Pump} and all the system regulators are over their under voltage rising threshold, S.A.B.Re enters in the normal operating state, that will release nRESET pin and will wait for SPI commands.

S.A.B.Re will reduce the noise introduced in the system by switching out of phase all its power circuits (switching regulators, bridges and charge pump).

The S.A.B.Re's startup sequence of operation is the following:

- start V_{3v3} internal linear regulator
- sample startup configuration
- wait enable if slave device
- start charge pump
- start system regulators (see order in *Section 8.7*)
- send enable to slave device, if master
- wait until V_{GPIO_SPI} becomes ok

10 Power saving modes

10.1 Overview

Saving power is very important for today platforms: S.A.B.Re implements different functions to achieve different levels of power saving.

Sections here below describe these different power saving modes.

10.2 Standby mode

Almost all low voltage circuitry inside S.A.B.Re are powered by V_{3v3} internal regulator; this regulator is a linear regulator powered by $V_{SupplyInt.}$ This means that all the current provided by V_{3v3} regulator is directly coming from $V_{SupplyInt}$ and therefore the total power consumption is:

$$\text{Low voltage power} = V_{Supply} * I_{V3v3}.$$

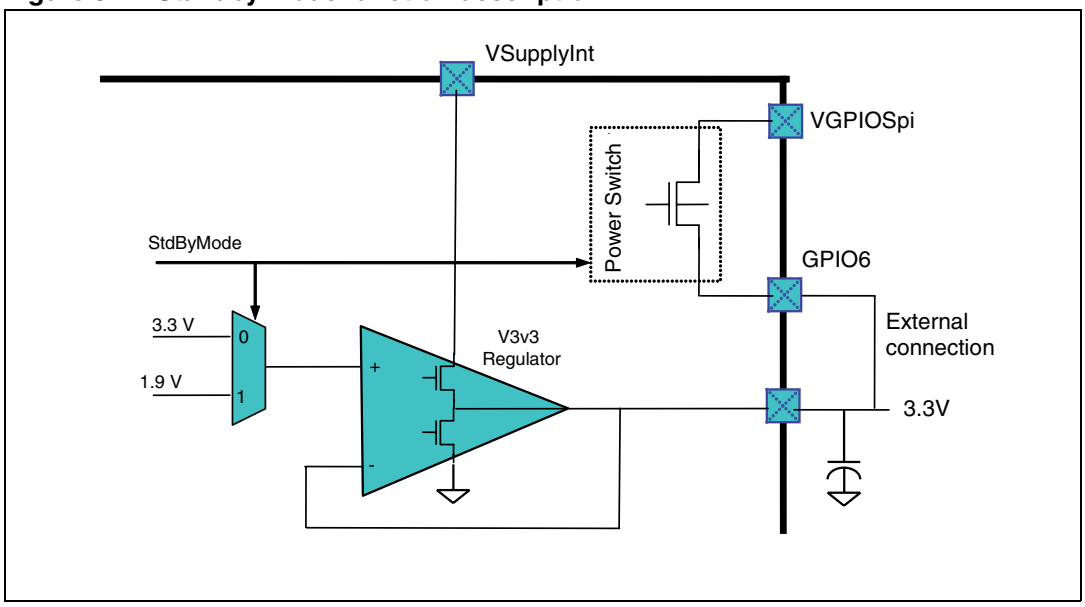
because $V_{SupplyInt}$ is feeded by V_{Supply}, directly or with a resistor in series.

This power could be reduced by using a switching buck regulator to supply V_{3v3}: in this case, assuming the buck regulator efficiency near to 100%, the dissipated power would become:

$$\text{Low voltage power} \approx 3.3V * I_{V3v3}.$$

To achieve this result there is the need to switch off the internal V_{3v3} linear regulator and to use an additional pin to provide a 3.3V supply to internal circuits. S.A.B.Re can do this by using the low voltage switch implemented on GPIO6 pin. This switch internally connects $V_{GPIOSpi}$ voltage to GPIO6 output so, by externally connecting GPIO6 to V_{3v3} pin, the $V_{GPIOSpi}$ voltage can be provided to low voltage circuitry inside S.A.B.Re.

Figure 5. Standby mode function description



The StdByMode bit used to switch off V_{3v3} and switch on the power switch can be set to '1' by writing the standby command in the StdByMode register. S.A.B.Re exits standby mode if a reset event happens or "Low Power mode" is selected.

Because all internal low voltage circuitry powered by V_{3v3} are designed to work with a 3.3V voltage rail, when the standby mode is used, $V_{GPIOSpi}$ is requested to be at 3.3V.

10.3 Hibernate mode

S.A.B.Re's hibernate mode allows the firmware to switch off some (or all) selected System Regulators leaving in on state only those necessary to resume S.A.B.Re to operative condition when waked-up by an external signal.

Hibernate mode is selected when the firmware writes the command word in the HibernateCmd register. When in hibernate mode S.A.B.Re will force regulators in the state (on/off) selected by the firmware by writing in the HibernateCmd register and will force nRESET pin low.

The exiting from hibernate mode is achieved by forcing at low level nAWAKE pin (or GPIO5 pin if S.A.B.Re is in Slave mode); S.A.B.Re will also exit from hibernate mode if an undervoltage event happens on V_{Supply}, $V_{SupplyInt}$, V_{Pump} or V_{3v3}.

When the exit from hibernate mode is due to an external command, S.A.B.Re sets to '1' the bit HibModeLth in the HibernateStatus register.

10.4 Low power mode

When in normal operating mode, the microcontroller can place S.A.B.Re in "Low Power mode".

In this condition S.A.B.Re sets all bridges outputs in high impedance, powers down all regulators (including system regulators and charge pump) and disables almost all its circuits including internal clock reducing as much as possible power consumption.

The only circuits that remain active are:

- V_{3V3} internal regulator.
- nAWAKE pin current pull-up.
- nRESET pin that will be pulled low.
- POR circuit.

The entering in low power mode is obtained in different ways depending if S.A.B.Re is configured as slave device or not. When S.A.B.Re is configured as slave device the low power mode is directly controlled by nAWAKE pin that acts as an enable: if this pin is low for a time longer then $t_{AWAKEFILT}$, Low Power mode is entered; if this pin is high S.A.B.Re exits from Low Power mode.

In all other start-up configurations, Low Power mode is entered by writing a Low Power mode command in the PowerModeControl register; once S.A.B.Re is in Low Power mode it starts checking the nAWAKE pin status: if it is found low for a time longer than $t_{AWAKEFILT}$, S.A.B.Re exits from Low Power mode and restarts its startup sequence. When the nAWAKE pin is externally pulled low, the "AWAKE" event is stored and it is readable through SPI. S.A.B.Re will also exit from Low Power mode if a POR event is found.

Note: When in "Low power mode" V_{Supply} is monitored only for its power on reset level.

10.5 nAWAKE pin

At the start up, before S.A.B.Re has identified the required operation mode (see *Chapter 8*), a current sink IINP is always active to pull down nAWAKE pin. As soon as the operation mode (basic, slave, master or single device) is detected, the functionality of nAWAKE pin will be different.

If S.A.B.Re is not configured as Slave device a current source IOUT will be active on this pin, while the current sink IINP will be disabled. If S.A.B.Re is configured as a Slave device, the current sink IINP will be active until nAWAKE pin is detected high for the first time; after that both current sources IINP and IOUT will be disabled and the nAWAKE pin can be considered as a digital input.

Here below is reported the nAWAKE pin simplified schematic.

Figure 6. nAWAKE function block diagram

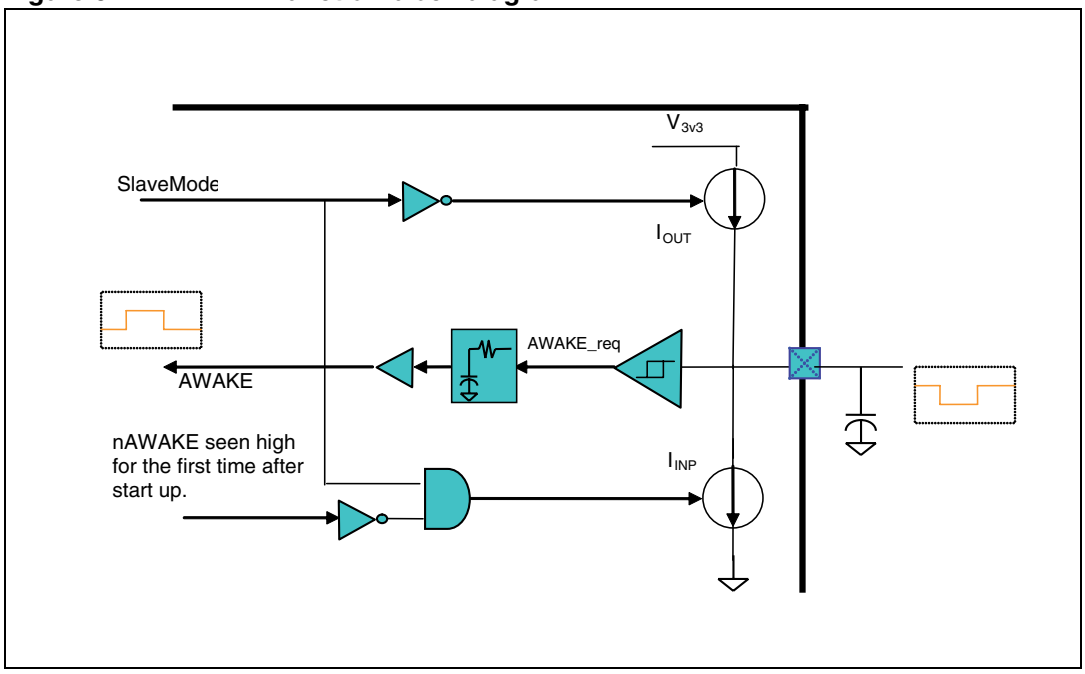


Table 16. nAWAKE function specifications

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IL}	nAWAKE logic low threshold				0.8	V
V_{IH}	nAWAKE logic high threshold		1.6			V
V_{HYS}	nAWAKE input hysteresys			0.25		V
I_{OUT}	nAWAKE pin output current	nAWAKE=0V(1)	- 0.72		- 2	mA
I_{INP}	nAWAKE pin input current	nAWAKE=0.8V(1)	0.2		0.4	mA
$t_{AWAKEFILT}$	Filter time			1.2		ns

1. Current is defined to be positive when flowing into the pin.

11 Linear main regulator

11.1 Overview

The linear main regulator is directly powered by V_{Supply} voltage and it is one of the regulators that S.A.B.Re could consider as a system regulator. This means that the voltage generated by this regulator is not used to power any internal circuit, but S.A.B.Re will check that the feedback voltage $V_{LINmain\_FB}$ is in the good value range before enabling all its internal functions. When an under-voltage event (with a duration longer than period T_{linear_uv} defined by the deglitch filter) is detected during normal operation, S.A.B.Re will enter in reset state and it will signal this event to the microcontroller by pulling low the nRESET pin and disabling most of its internal blocks.

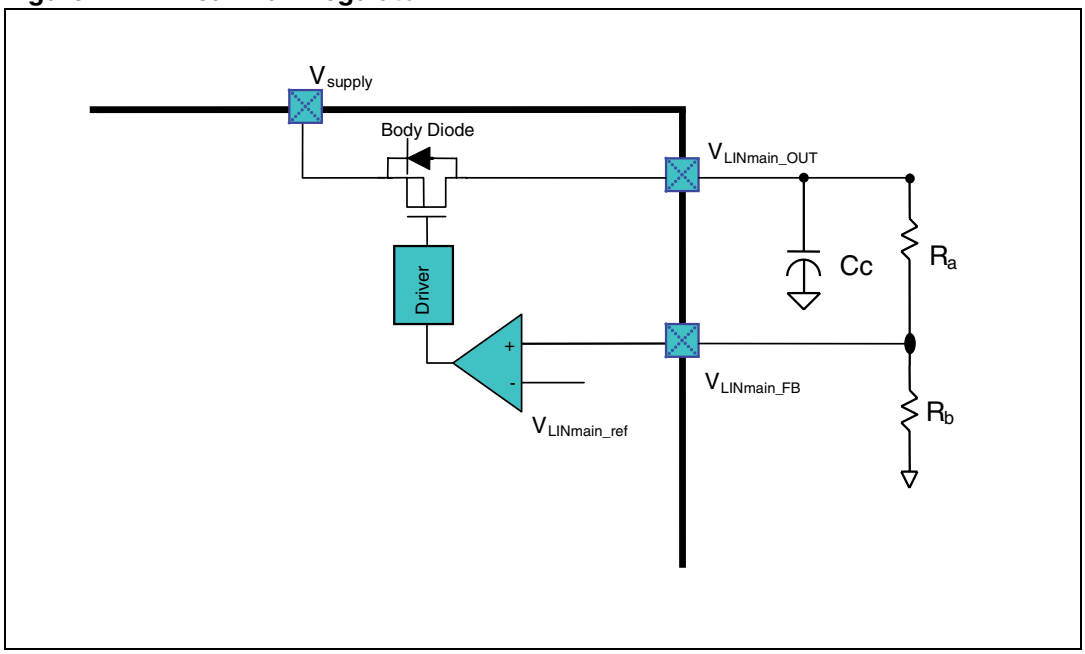
Here are summarized the primary features of the regulator:

- Regulated output voltage from 0.8V to V_{Supply}-2V with a maximum load of 10mA.
- Band gap generated internal reference voltage.
- Short circuit protected (output current is clamped to 22mA typ).
- Under voltage signal (both continuous and latched) accessible through serial interface.
- Low power dissipation mode.

The internal series element is a P-channel MOS device. The voltage regulator will regulate its output so that feedback pin equals $V_{LINmain\_FB}$, therefore the regulated voltage can be calculated using the formula:

$$V_{LINmain\_OUT} = V_{LINmain\_ref} *(Ra+Rb)/Rb$$

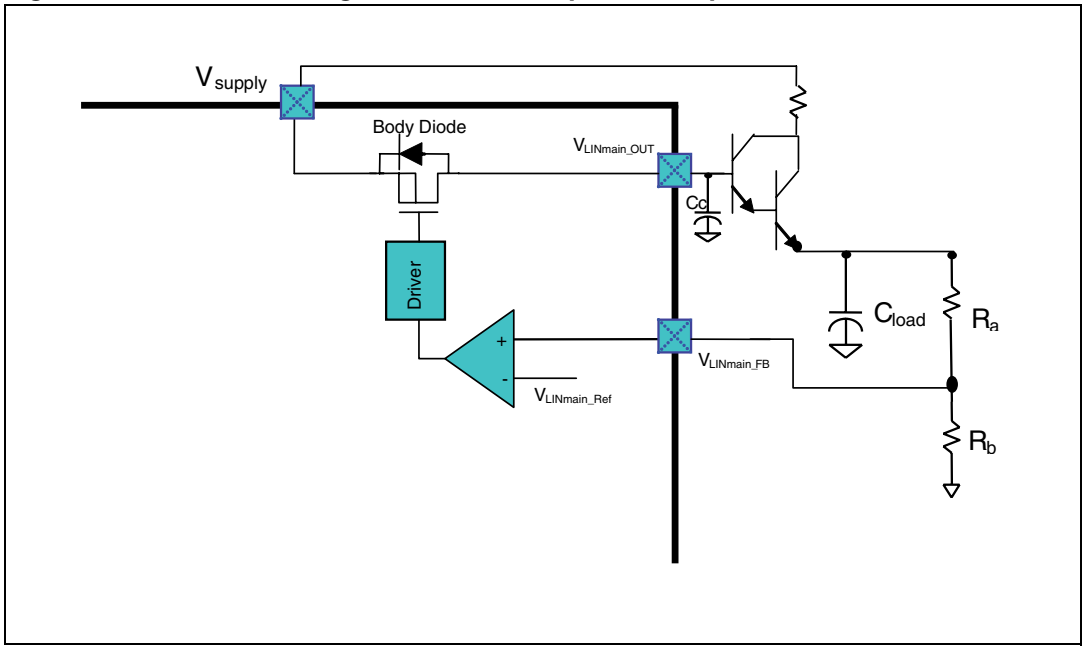
Figure 7. Linear main regulator



To extend the output current capability this regulator can be used as a controller for an external active component able to provide higher current (i.e. a Darlington device); the external power element allows the handling of an higher current since it dissipates the

power externally (the power dissipated by a linear driver supplied at V_{Supply} and regulating a voltage $V_{LINmain\_OUT}$ with an output current I_{OUT} is about: Pd= $(V_{Supply}-V_{LINmain\_OUT})*I_{OUT}$.

Figure 8. Linear main regulator external bipolar example



Whichever configuration is used (regulator or controller), a ceramic capacitor must be connected on the output pin towards ground to guarantee the stability of the regulator; the value of this capacitance is in the range of 100nF to 1µF depending on the regulated voltage.

When this regulator is disabled, the whole circuit is switched off and the current consumption is reduced to a very low level both from V3v3 and from V_{Supply}. When in this condition, the output pin is pulled low by an internal switch.

Table 17. System linear regulator operating specifications

Parameter	Description	Test condition	Min	Typ	Max	Unit
$V_{LINmain\_OUT}$	Output pin voltage range	(1)	0		V_{Supply}	V
V_{drop}	Drop out voltage	V_{drop}= V_{supply}-$V_{LINmain\_OUT}$	2			V
I_{PD}	Internal switch pull down current	Linear Main Regulator disabled; $V_{LINmain\_OUT}$=1V		3		mA
$V_{LINmain\_FB}$	Feedback pin voltage range		0		3.6	V
$V_{LINmain\_Ref}$	Feedback reference voltage		0.776	0.8	0.824	V
$I_{LINmain\_Ref}$	Feedback pin input current		-2		2	µA

Table 17. System linear regulator operating specifications (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
$I_{outLinMax}$	Maximum Output current	Regulated voltage = V_{supply}-2V	10			mA
I_{short}	Output short circuit current	$V_{LINmain\_OUT}$ =0V, $V_{LINmain\_FB}$ =0V	12	24		mA
$\Delta V_{out}/V_o$	Load regulation	$0 \leq I_{load} \leq I_{outLinMax}$ (2)			0.8	%
$\Delta V_{out}/\Delta V_{Supply}$	Line regulation	I_{load} =10mA (2)			0.2	%
V_{loop_acc}	Loop voltage accuracy			±2.5		%
V_{uvFall}	Under voltage falling threshold	(3)	84.5	87	89.5	%
V_{uvRise}	Under voltage rising threshold	(3)	90.5	93	95.5	%
V_{uvhys}	Under voltage hysteresis	(3)		6		%
t_{prim_uv}	Under voltage deglitch filter			5		us
C_C	Compensation capacitance	$V_{LINmain\_OUT}$ =0.8V 0.8V<$V_{LINmain\_OUT}$ < 2.5V 2.5V=$V_{LINmain\_OUT}$ ≤ 5V $V_{LINmain\_OUT}$ > 5V		1 0.68 0.33 0.1		µF

1. The external components connected to the pin must be chosen to avoid that the voltage exceeds this operative range.
2. Load regulation is calculated at a fixed junction temperature using short load pulses covering all the load current range. This is to avoid change on output voltage due to heating effect.
3. Undervoltage rising and falling thresholds are intended as a percentage of feedback pin voltage ($V_{LINmain\_Ref}$).

12 Main switching regulator

12.1 Overview

Main switching regulator is an asynchronous switching regulator intended to be the source of the main voltage in the system. It implements a soft start strategy and could be a system regulator so even if its output voltage V_{MAIN_SW} is not used to power any internal circuit, S.A.B.Re will check that it is in the good value range before enabling all its internal functions. When S.A.B.Re detects a system regulator under-voltage event with a duration longer than the period defined by the deglitch filter (T_{prim_uv}), it will enter in reset state signaling this event to the microcontroller by pulling low the nRESET pin and disabling most of its internal block (e.g. bridges, GPIOs, …).

The output voltage will be externally set by a divider network connected to feedback pin. To reduce as much as possible the regulation voltage error S.A.B.Re has the possibility to choose between four feedback voltage references (and, as a consequence, four under-voltage thresholds) using the serial interface. The feedback reference voltage selection is made by writing the SelFBRef bits in the MainSwCfg register according to the table here below:

Table 18. Switching regulator controller PWM specification

MainSwCfg register		Reference voltage (V_{FBREF})			Unit	Comments
SelFBref[1]	SelFBref[0]	Min	Typ	Max		
0	0	0.776	0.8	0.824	V	
0	1	0.97	1	1.03	V	Default state
1	0	2.425	2.5	2.575	V	
1	1	2.910	3	3.09	V	

Reference voltage range can be changed by using a metal layer change in order to adapt them to customer system.

Here after are summarized the primary features of this regulator:

- Internal power switch.
- Soft start circuitry to limit inrush current flow from primary supply.
- Internally generated PWM (250kHz switching frequency).
- Nonlinear pulse skipping control.
- Protected against load short circuit.
- Cycle by cycle current limiting using internal current sensor.
- Under voltage signal (both continuous and latched) accessible through SPI.

When S.A.B.Re is in “Low Power mode”, this regulator will be disabled.

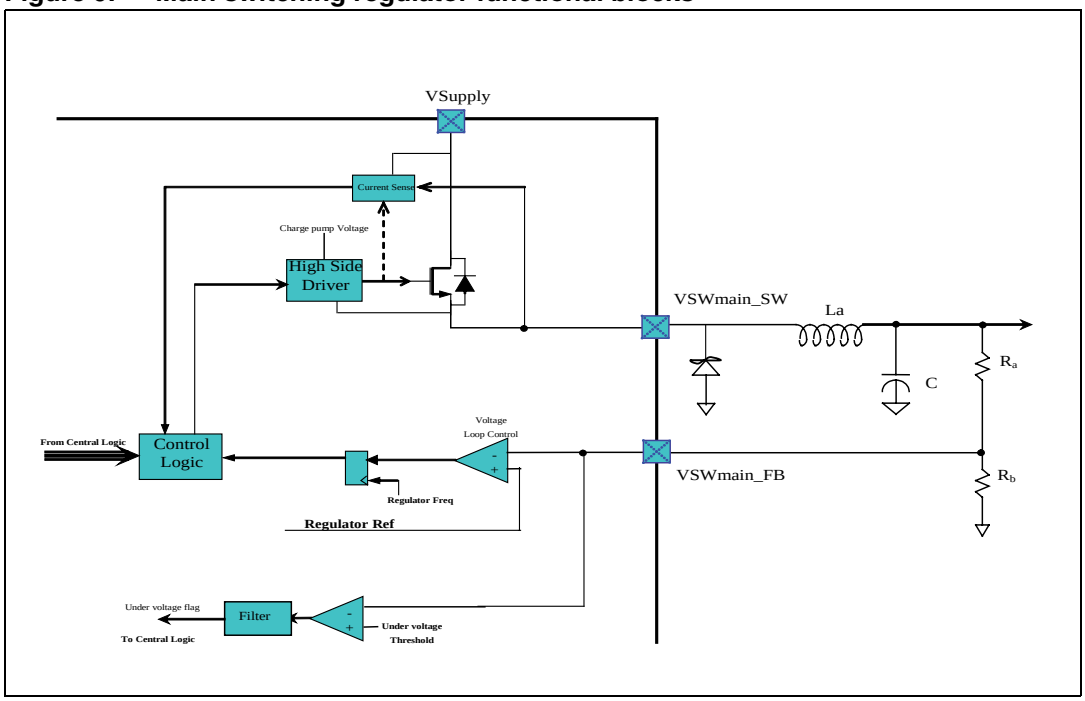
In order to save external components and power when using two or more S.A.B.Re IC’s on the same board, the primary switching regulator can be disabled by serial interface. Care must be paid using this function because an under-voltage on this regulator, as previously seen, will be read as a fault condition by S.A.B.Re.

12.2 Pulse skipping operation

Pulse skipping is a well known, non linear, control strategy used in switching regulators.

In this technique (see *Figure 9*) the feedback comparator output is sampled at the beginning of each switching cycle. At this time, if the sampled value shows that output voltage is lower than requested one, the complete PWM duty cycle is applied to power switch; otherwise no PWM is applied and the switching cycle is skipped. Once PWM is applied to power element only a current limit event can disable the power switch before the whole duty cycle is finished.

Figure 9. Main switching regulator functional blocks



In pulse skipping control the duty cycle must be chosen by the user depending on supply voltage and output regulated voltage. Therefore the switching regulator has 4 possible duty cycles that can be changed by writing the VmainSwSelPWM bits in the MainSwCfg register according to following table.

Table 19. Main switching regulator PWM specification

MainSwCfg register	Duty cycle value	Comments
VmainSwSelPWM[1:0]	Typical	
00	12%	
01	15%	
10	26%	Default state
11	63.5%	

Adjustable duty cycles can be changed by a metal layer change in order to adapt it to customer system. The only limitation is that all regulators share the same duty cycle bus, so any modification must consider all regulators duty cycles.

The output current is limited to a value that can be set by means of selilimit bit in the MainSwCfg register according to following table:

Table 20. Main switching regulator current limit

Selllimit	Current limit (min)	Comments
0	3.3A	Default state
1	2.3A	

Table 21. Main switching regulator specifications

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{MAIN_SW}	Output pin voltage range	(1)	-1		V_{supply}	V
I_Q	Output leakage current	$T_{junction}$ = 125°C	-40		+40	µA
I_{Qlp}	Output leakage current in "Low Power Mode"	V_{Supply} = 36V $T_{junction}$ = 125°C	-15		+5	µA
I_{Qfb}	Feedback pin current	$T_{junction}$ = 125°C	-10		+0	µA
V_{out}	Output voltage range	(2)	0.8		5	V
I_{load}	Output load current	V_{Supply} = 36V	0.002		3	A
R_{onH}	Internal high side RDson	Iload=1A $T_{junction}$ = 125°C			0.55	O
V_{loop}	Loop voltage accuracy			±3%		
V_{regR}	Output voltage ripple (RMS)	L =150u, C=330µF/ESR=0.54Ω (3)		28		mV_{RMS}
V_{uvFall}	Under voltage falling threshold	(4)	84.5	87	89.5	%
V_{uvRise}	Under voltage rising threshold	(4)	90.5	93	95.5	%
V_{uvhys}	Under voltage hysteresys			6		%
t_{prim_uv}	Under voltage deglitch filter			5		us
I_{limit}	Current limit protection	Selllimit ="0" Selllimit ="1"	3.3 2.3	5 3.5	TBD TBD	A A
$t_{deglitch}$	Current limit deglitch time		50			ns
t_{I_lim}	Current limit response time	In normal operating mode (no UV)(5)			650	ns
t_{I_limUV}	Current limit response time in UV condition.	When in Under Voltage(6)			400	ns
t_r	Switching output rise time	V_{Supply} = 36V, Resistive load to gnd = 422 Ω(7)	5		30	ns
t_f	Switching output fall time	V_{Supply} = 36V, Resistive load to gnd = 10 Ω(7)	5		30	ns
F_{regPwm}	Operating frequency			Fosc/64		kHz

1. The external components connected to the pin must be chosen to avoid that the voltage exceeds this operative range.
2. The regulated voltage can be calculated using the formula: $V_{MAIN\_SW = VFBREF}$ *(Ra+Rb)/Rb.
3. The choice of proper values for L and C depends from the application.
4. Undervoltage rising and falling thresholds are intended as a percentage of feedback pin voltage ($V_{SW\_main\_FB}$).
5. This condition is intended to simulate an extra current on output.
6. This condition is intended to simulate a short circuit on output.
7. Rise time is measured between 10% and 90% of supply voltage.

13 Switching regulator controller

13.1 Overview

This circuit controls an external FET to implement a switching buck regulator using a non linear pulse skipping control with internally generated PWM signal.

The output voltage will be externally set by a divider network connected on feedback pin. To reduce as much as possible the regulation voltage error S.A.B.Re has the possibility to switch between four regulator feedback voltage references (and, as a consequence, four under-voltage thresholds) using serial interface. The feedback reference voltage is selected by writing the SelFBRef bits in the SwCtrCfg register according to the following table.

Table 22. Switching regulator controller PWM specification

SwCtrCfg register		Reference voltage (V_{FBREF})			Unit	Comments
SelFBref[1]	SelFBref[0]	Min	Typ	Max		
0	0	0.776	0.8	0.824	V	Default state
0	1	0.970	1	1.030	V	
1	0	2.425	2.5	2.575	V	
1	1	2.910	3	3.09	V	

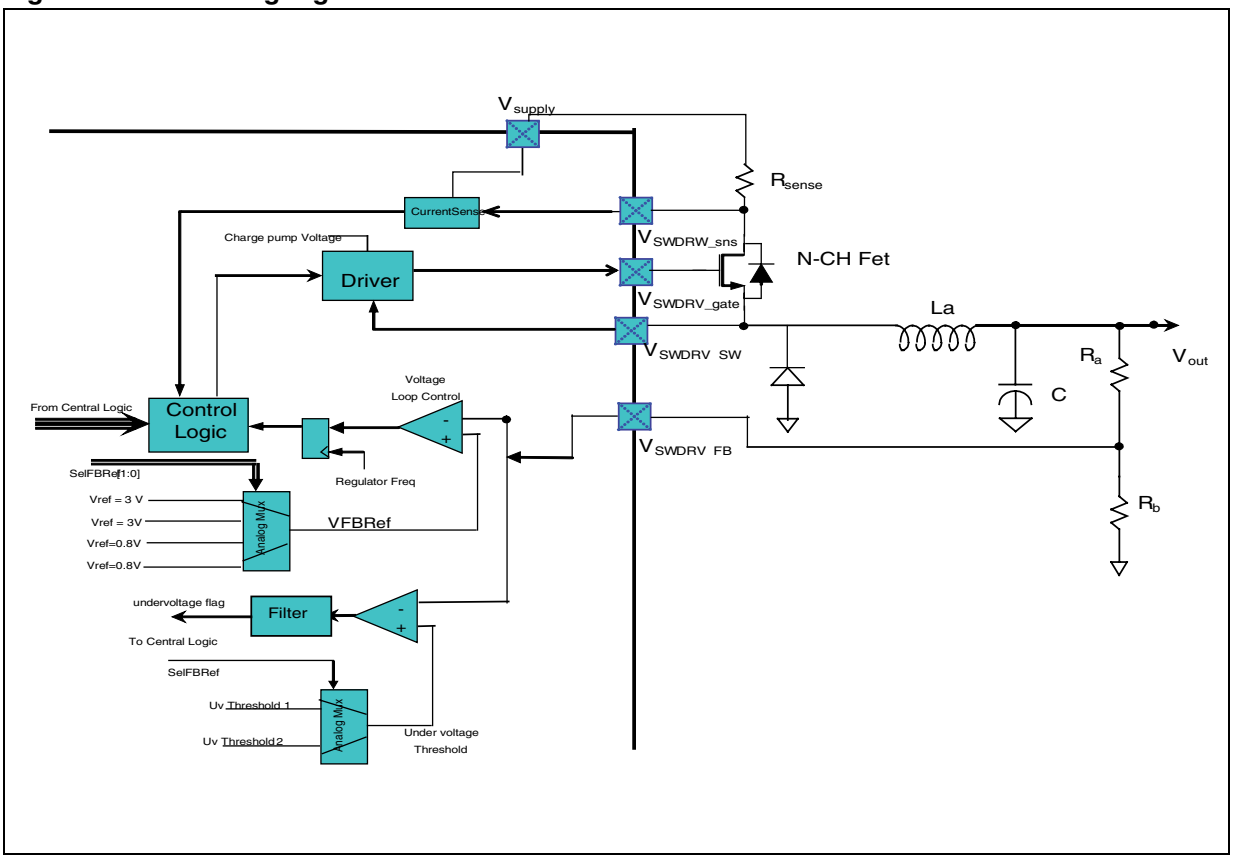
Adjustable feedback voltages can be changed using a metal layer change in order to adapt it to customer system.

This regulator is switched off when S.A.B.Re is powered up for the first time and can be enabled using S.A.B.Re's SPI interface.

Here after are summarized the main features of the regulator:

- Soft start circuitry to limit inrush current flow from primary supply.
- Changeable feedback reference voltage
- Internally generated PWM (250kHz switching frequency).
- Nonlinear pulse skipping control.
- Protected against load short circuit.
- Cycle by cycle current limiting using internal current sensor.
- Under voltage signal (both continuous and latched) accessible through SPI.

Figure 10. Switching regulator controller functional blocks



13.2 Pulse skipping operation

Pulse skipping strategy has already been explained on main switching regulator section.

This regulator has 4 possible PWM duty cycles that can be changed writing in the SelSwCtrPWM bits in the SwCtrCfg register using SPI.

Table 23. Switching regulator controller PWM specification

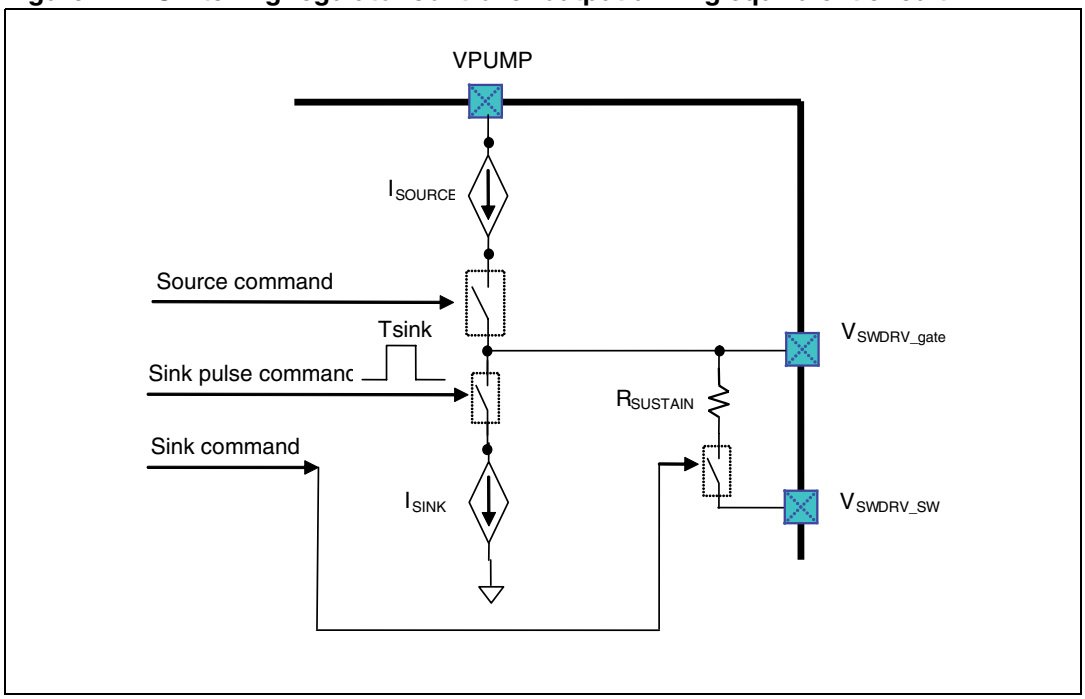
SwCtrCfg register	Duty cycle value	Comments
SelSwCtrPWM[1:0]	Typical	
00	9%	
01	12%	
10	22.5%	Default state
11	58%	

Adjustable duty cycles can be changed using a metal layer change in order to adapt it to customer system. The only limitation is that all regulators share the same duty cycle bus, so any modification must consider all regulators needed duty cycles.

13.3 Output equivalent circuit

The switching regulator controller output driving stage can be represented with an equivalent circuit as in the figure below:

Figure 11. Switching regulator controller output driving equivalent circuit



As can be seen from the above figure, the external switch gate is charged with a current generator I_{SOURCE} and it is discharged towards ground with a current generator I_{SINK} that is applied for a T_{SINK} pulse while an equivalent resistor $R_{SUSTAIN}$ is connected between gate and source until the sink command is present.

The table here below lists the values of the above mentioned parameters:

Table 24. Switching regulator controller operating specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
I_{SOURCE}	Source current	$V_{Pump}=V_{Supply}+12V$ $V_{SWCTR\_GATE}=0V$	25		50	mA
I_{SINK}	Sink current	$V_{SWCTR\_GATE} = V_{Supply}$	20			mA
t_{SINK}	Sink discharge pulse time			600		ns
$R_{SUSTAIN}$	Gate-source sustain resistance	$(V_{SWCTR\_GATE} - V_{SWCTR\_SRC})$ = 0.2V		650		Ω

13.4 Switching regulator controller specifications

Table 25. Switching regulator controller operating specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{SWDRV_SW}	V_{SWDRV_SW} pin voltage range	(1)	-1		V_{Supply}	V
V_{SWDRV_GATE}	Gate drive pin voltage		0		V_{Pump}	V
V_{SWDRV_SNS}	Sense pin voltage		V_{Supply} -3V		V_{Supply}	V
V_{vgs_ext}	Gate to source voltage for ext FET			V_{Pump}		V
I_Q	Output leakage current	V_{Supply} = 36V, $T_{junction}$ = 125°C	-15		+15	µA
I_{Qlp}	Output leakage current in “Low Power Mode”	V_{Supply} = 36V, $T_{junction}$ = 125°C	-5		+5	µA
V_{SWDRV_FB}	V_{SWDRV_FB} pin current	V_{Supply} = 36V, $T_{junction}$ = 125°C	-10		+10	µA
V_{loop}	Loop voltage accuracy			±3%		
V_{uvFall}(1)	Under voltage falling threshold		84.5	87	89.5	%
V_{uvRise}(1)	Under voltage rising threshold		90.5	93	95.5	%
V_{uvhys}(1)	Under voltage hysteresys			6		%
t_{prim_uv}	Under voltage deglitch filter			5		us
V_{ovc}	Over current threshold voltage		250	300	350	mV
$t_{deglitch}$	Current limit deglitch time		50			ns
t_{I_lim}	Current limit response time	In normal operating mode (no UV)(2)			900	ns
t_{I_limUV}	Current Limit response time in UV condition.	When in Under Voltage(3)			550	ns
F_{regPwm}	Operating frequency			Fosc/64		kHz

1. Under voltage rising and falling thresholds are referred to feedback pin voltage.
2. This condition is intended to simulate an extra current on output.
3. This condition is intended to simulate a short circuit on output.

13.5 Switching regulator controller application considerations

This controller can implement a step-down switching regulator used to provide a regulated voltage in the range 0.8V – 32V. Such kind of variation could be managed by considering

some constraints in the application and particularly by choosing the correct feedback reference voltage as indicated in the following table:

Table 26. Switching regulator controller application feedback reference

Output regulated voltage range	Feedback voltage reference
$0.8V \leq V_{out} < 5V$	0.8V - 1V
$5V \leq V_{out} \leq 32V$	2.5V - 3V

Typical application can be considered the following, supposing the external mosfet type STD12NF06L:

- Max DC current load = 3A
- Typ Over current threshold = 3A * 1.5 = 4.5A
- L = 150 µH
- C = 220-330 µF

In this conditions the step-down regulator will result over-load protected, short-circuit protected over all the regulated voltage range and the V_{Supply} range.

Other application configurations could be evaluated before being implemented.

14 Power bridges

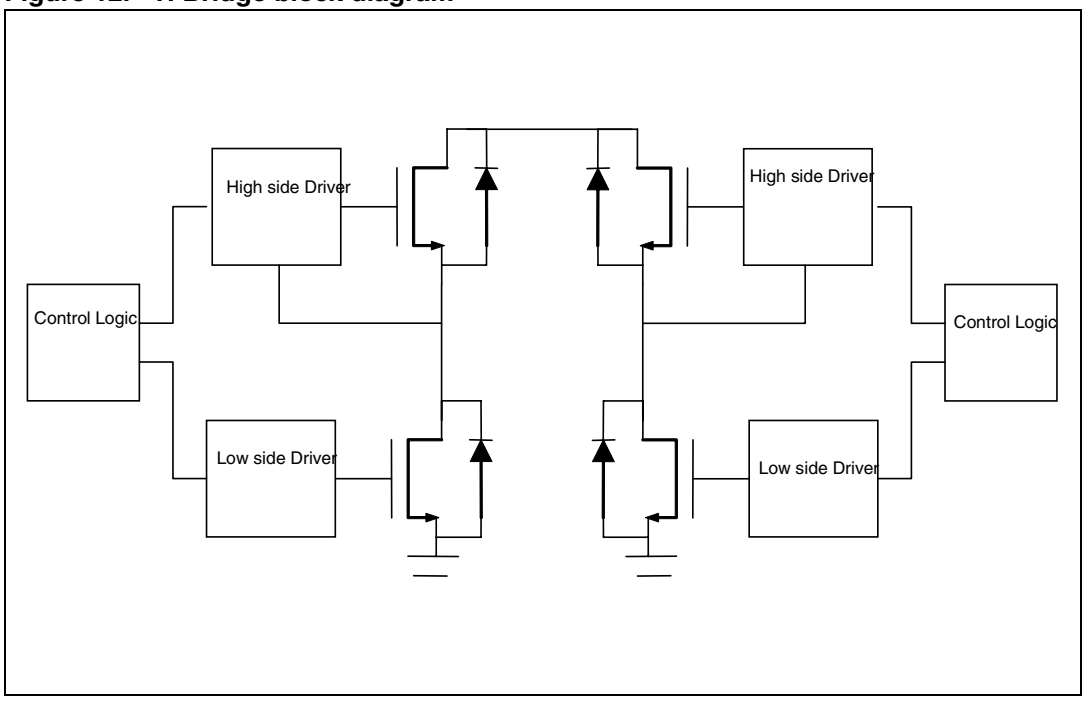
14.1 Overview

S.A.B.Re includes four H bridge power outputs (each one made by two independent half bridges) that are configurable in several different configurations.

Each half bridge is protected against: over-current, over-temperature and short circuit to ground, to supply or across the load. When an over current event occurs, all outputs are turned off (after a filter time), and the over current bit is stored in the internal status register that can be read through SPI.

Positive and negative voltage spikes, which occur when switching inductive loads, are limited by integrated freewheeling diodes (see *Figure 12*).

Figure 12. H Bridge block diagram



During the start up procedure the bridges are in high impedance and after that they can be enabled through SPI. When a fault condition happens, i.e. an over-temperature event, the bridges return in their start-up condition and they need to be re-enabled from the micro controller.

The bridges can use PWM signals internally generated or externally provided (supplied through the GPIO pins). Internally generated PWM signals will run at approximately 31.25kHz with a duty cycle that, through serial interface, can be programmed and incremented in steps of 1/(512*Fosc). To reduce the peak current requested from supply voltage when all bridges are switching, the four internally generated PWM signals are out-of-phase.

Each half bridge will use the PWM signal selected by the respective MtrXSelPWMSideY[1:0] (X stands for 1, 2, 3 or 4; Y stands for A or B) bits in the SPI, but if

two half bridges are configured as a full bridge, only the PWM signal chosen for side A will be used to drive the resulting H bridge.

More in detail the PWM selection truth table will be as describe in the following tables:

Table 27. PWM selection truth for bridge 1 or 2

MtrXSelPWMSideY [1]	MtrXSelPWMSideY [0]	Selected PWM(1)
0	0	MotorXPWM (Configurable by means of MtrXCfg register).
0	1	AuxXPWM (Configurable by means of AuxPwmXCtrl register).
1	0	ExtPWM1 (from GPIO 9 input)
1	1	ExtPWM2 (from GPIO 10 input)

1. In this table X stands for 1 or 2, Y stands for A or B.

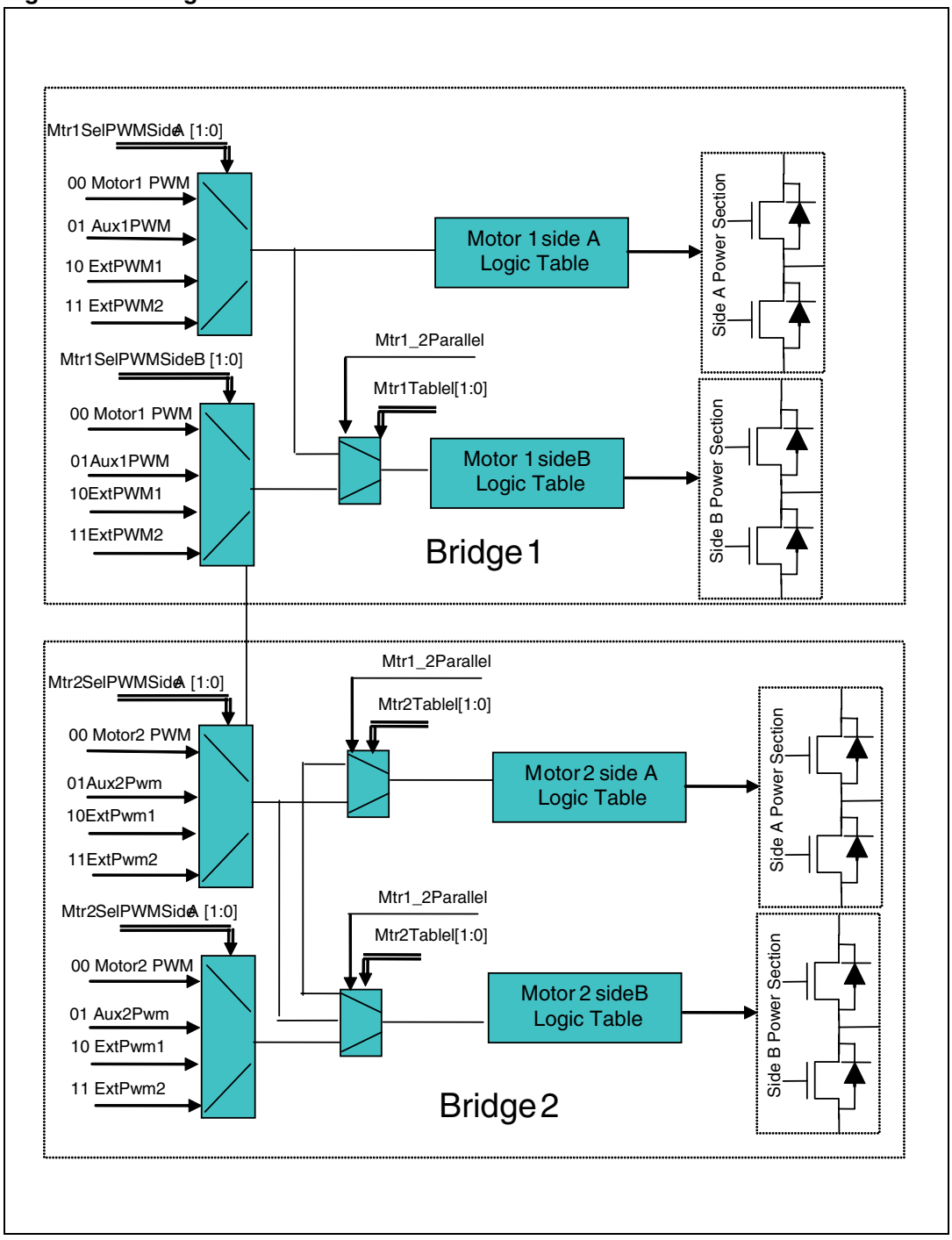
Table 28. PWM selection truth for bridge 3 or 4

MtrXSelPWMSideY [1]	MtrXSelPWMSideY [0]	Selected PWM(1)
0	0	MotorXPWM (Configurable by means of MtrXCfg register).
0	1	AuxXPWM (Configurable by means of AuxPwmXCtrl register).
1	0	ExtPWM3 (from GPIO 2 input)
1	1	ExtPWM4 (from GPIO 11 input)

1. In this table X stands for 3 or 4, Y stands for A or B.

Here below is reported a block diagram representing the possible PWM choices for each S.A.B.Re half bridges. The figure is related only to bridges 1 and 2, but it could be assumed to be valid also for bridges 3 and 4, with few differences due to different possible configurations of these last drivers.

Figure 13. Bridge 1 and 2 PWM selection



14.2 Power bridges operating specifications

Table 29. Power bridges operating specifications

Parameter	Description	Test condition	Min	Typ	Max	Unit
$R_{ON\_1\_2}$	Bridge 1 and 2 diagonal Ron	I = 1.4A, V_{Supply} = 36V, $T_{junction}$ = 125°C			1.0	Ω
$R_{ON\_3\_4}$	Bridge 3 and 4 diagonal Ron	I = 1A, V_{Supply} = 36V, $T_{junction}$ = 125°C			1.5	Ω
I_{Max}	Bridge 1 and 2 max operative current				2.5	A
I_{Max}	Bridge 3 and 4 max operative current				1.5	A
I_{dss}	Output leakage current.	$T_{junction}$ = 125°C	-50		+50	µA
I_{Qlp}	Output leakage current in “Low Power Mode”	V_{Supply} = 36V, $T_{junction}$ = 125°C	-10		+10	µA
$I_{protL\_1\&2}$	Low side current protection for bridges 1 & 2(1)	MtrXSideYILimSel[1:0]=00 MtrXSideYILimSel[1:0]=01 MtrXSideYILimSel[1:0]=10 MtrXSideYILimSel[1:0]=11(2)	0.6 1.4 2.4 2.4		1.6 2.6 3.6 3.6	A
$I_{protH\_1\&2}$	High side current protection for bridges 1 & 2(1)	MtrXSideYILimSel[1:0]=00 MtrXSideYILimSel[1:0]=01 MtrXSideYILimSel[1:0]=10 MtrXSideYILimSel[1:0]=11(2)	0.7 1.5 2.5 2.5		1.7 2.7 3.7 3.7	A
I_{prot_3}	Low side current protection for bridges 3 & 4(1)	MtrXSideYILimSel[1:0]=11(3)(4)	1.55		2.5	A
I_{prot_4}	High side current protection for bridges 3 & 4(1)	MtrXSideYILimSel[1:0]=11(3)(4)	1.6		2.5	A
t_{filter}	Current limit filter time		2		5	us
t_{delay}	Current limit delay time			5		us
t_{oc_off}	Over current off time	MtrXIlimitOffTimeY[1:0]=00 MtrXIlimitOffTimeY[1:0]=01 MtrXIlimitOffTimeY[1:0]=10 MtrXIlimitOffTimeY[1:0]=11(5)		60 120 240 480		ns ns ns ns
t_{r1_2}	Output rise time bridges 1 &2	V_{Supply} = 36V, Resistive load between outputs: R= 25 Ohm(6)	100		250	ns
t_{r3_4}	Output rise time bridges 3 & 4	V_{Supply} = 36V, Resistive load between outputs: R= 36 Ohm(6)	50		200	ns
t_{f1_2}	Output fall time bridges 1 & 2	V_{Supply} = 36V, Resistive load between outputs: R= 25 Ohm(6)	100		250	ns

Table 29. Power bridges operating specifications (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
t_{f3_4}	Output fall time bridges 3 & 4	V_{Supply} = 36V, Resistive load between outputs: R= 36 Ohm(6)	50		250	ns
$t_{deadRise}$	Anti crossover rising dead time		100		450	ns
$t_{deadFall}$	Anti crossover falling dead time		100		450	ns
F_{pwm}	Operating frequency			Fosc /512		kHz
t_{resp}	Delay from PWM to output transition			500		ns

1. The current protection values must be intended as a protection for the chip and not as a continuous current limitation. The protection is performed by switching off the output bridge when current reaches values higher than the Iprot max. No protection could be guaranteed for values in the middle range between Ioperative max and Iprot.
2. In this cell X stands for 1 or 2, Y stands for A or B
3. In this cell X stands for 3 or 4, Y stands for A or B
4. The current protection thresholds for Bridge 3 and 4 are not selectable so only the max current value (MtrXSideYILimSel[1:0]= 11) is available.
5. Over Current Off time can be configured using SPI.
6. Rise and fall time are measured between 10% and 90% of supply voltage. With device in full bridge configuration (resistive load between outputs).

14.3 Possible configurations

The selection of the bridge configuration is done through SPI, by writing the MtrXTable[1:0] bits in the MtrXCfg register. The table below shows the correspondence between MtrXTable[1:0] bits and the bridge configuration.

Table 30. Bridge selection truth

MtrXTable[1]	MtrXTable[0]	Bridge truth
0	0	Full bridge configuration
0	1	High or low side switch configuration
1	0	Half bridge configuration
1	1	High or low side switch configuration

Bridge 1 & 2 can be paralleled by means of Mtr1_2Parallel bit in the Mtr1_2Cfg register: Bridge 1 and 2 paralleled will form superbridge1, bridge X side A and bridge X side B paralleled form SuperHalfBridgeX or SuperSwitchX.

Bridge 3 & 4 can be configured by means of Mtr3_4CfgTable[1:0] bits in the Mtr3_4Cfg register according to following table:

Table 31. Bridge 3 and 4 configuration

Mtr3_4CfgTable[1]	Mtr3_4CfgTable[0]	Bridge 3 and 4 configuration
0	0	Two independent bridges
0	1	Two bridges in parallel
1	0	Stepper motor
1	1	Stepper motor

The possible configurations for the bridges are described in the following:

14.3.1 Full bridge

When in full bridge configuration, the drivers will behave according to the following truth table:

Table 32. Full bridge truth

TSD	nRESET	Low power mode	Enable	Current limit	MtrXCtrl SideA	MtrXCtrl SideB	PWM	OUT+	OUT-
1	X	X	X	X	X	X	X	Z	Z
0	0	X	X	X	X	X	X	Z	Z
0	1	1	X	X	X	X	X	Z	Z
0	1	0	0	X	X	X	X	Z	Z
0	1	0	1	1	X	X	X	Z	Z
0	1	0	1	0	0	0	X	0	0
0	1	0	1	0	0	1	0	1	1
0	1	0	1	0	0	1	1	0	1
0	1	0	1	0	1	0	0	1	1
0	1	0	1	0	1	0	1	1	0
0	1	0	1	0	1	1	X	1	1

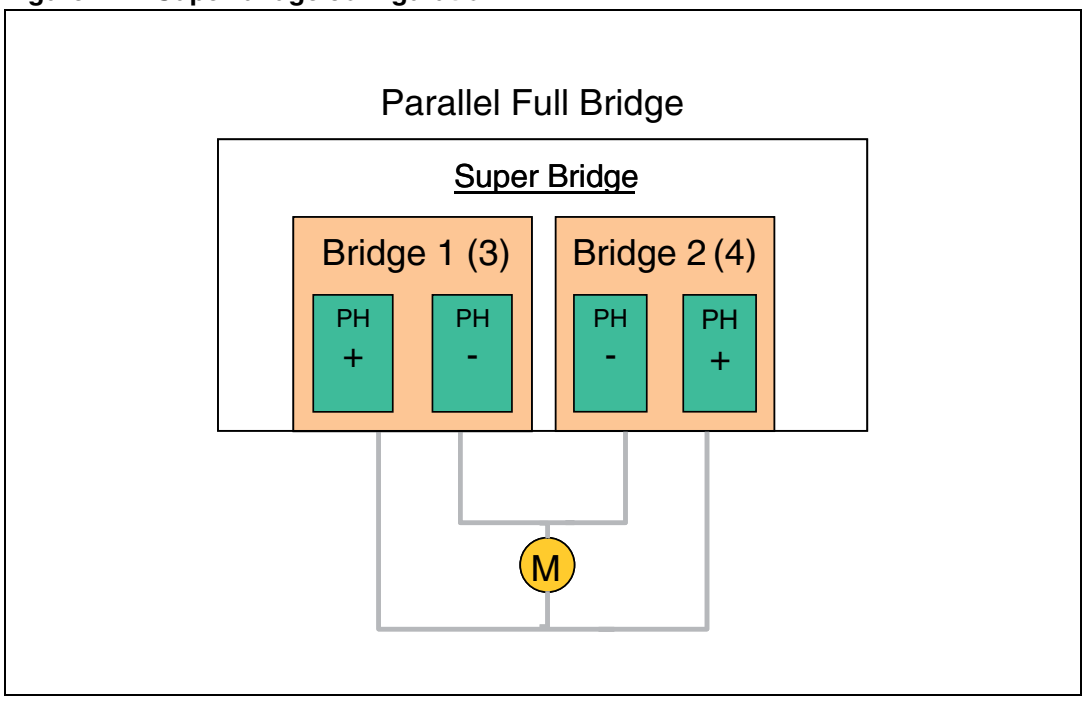
Note: When “Low Power mode” is active, the bridges will enter in low power state and will reduce its biasing thus contributing to the power saving.

When a current limit event occurs this event will be latched and the bridges will remain in high impedance state for the toff time.

14.3.2 Parallel configuration (super bridge)

Bridges 1, 2, 3 and 4 can be configured to be used two by two (1 plus 2, 3 plus 4) as one super bridge thus enabling the driving of loads (motors) requiring high currents. In this configuration the half bridges will be paralleled and will work as one phase of the super-bridge just created: the two phases + will become phase + of the newly created super-bridge while the two phases - will become phase –.

Figure 14. Super bridge configuration



When this configuration is chosen for bridges 1 (3) and 2 (4), the resulting bridge will use the driving logic of bridge 1 (3) so for programming it must be used the bridge 1 (3) control and status bits (direction, PWM, ...): i.e. the used PWM signal will be chosen by Mtr1SideAPwmSel[1:0] (Mtr3SideAPwmSel[1:0]) bits in SPI.

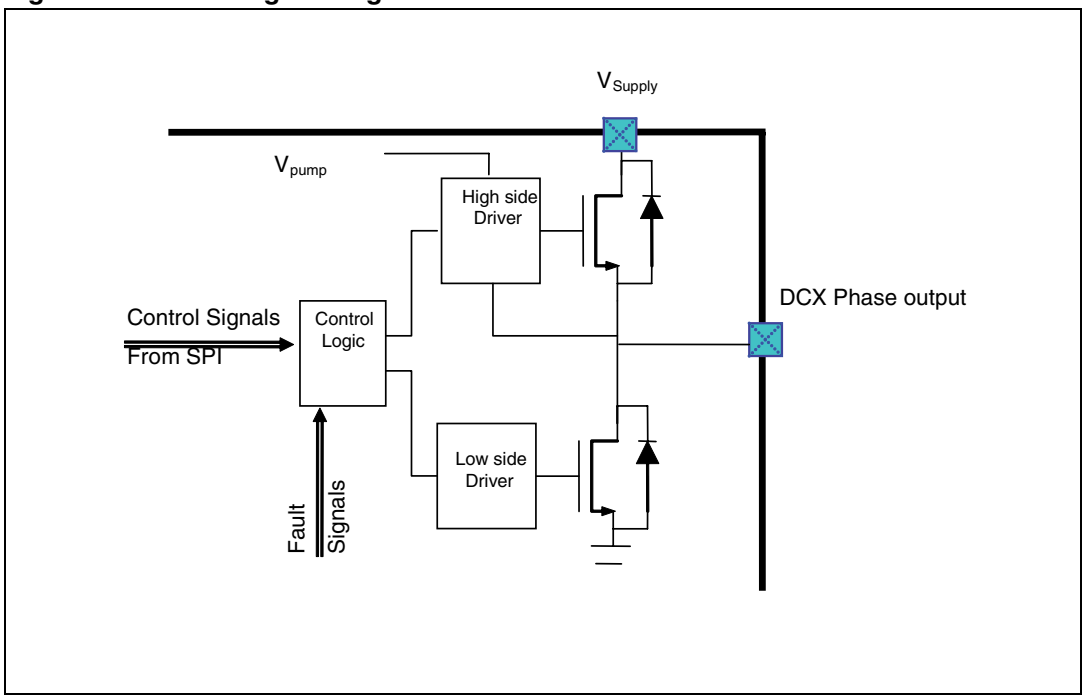
If the bridges are not configured to be used in parallel, each side of the bridge will use the PWM selected by the respective MtrXPWMYSel[1:0] bits in the SPI, but if one of the two drivers is configured as a full bridge only one of the two selected PWM will be used to drive the motor and this is the PWM chosen for side A.

In order to avoid any problem coming from different propagation times of PWM signals the anti-crossover dead times are slightly increased when the bridges are paralleled.

14.3.3 Half bridge configuration

Each bridge can be configured to be used as 2 independent half bridges or as 1 super half bridge (see *Figure 15*). It is also possible to parallel more than one bridge and use all of them as a single super half bridge.

Figure 15. Half bridge configuration



In this case each half bridge will behave according to the following truth table.

Table 33. Half bridge truth

TSD	nReset	Low power mode	Enable	Current limit	MtrXCtrl SideA/B	PWM	OUT
1	X	X	X	X	X	X	Z
0	0	X	X	X	X	X	Z
0	1	1	X	X	X	X	Z
0	1	0	0	X	X	X	Z
0	1	0	1	0	0	0	Z
0	1	0	1	0	0	1	0
0	1	0	1	0	1	0	Z
0	1	0	1	0	1	1	1
0	1	0	1	1	X	X	Z

Note: When “Low Power mode” bit is active the bridges will reduce its biasing thus contributing to the power saving.

When a current limit event occurs this event will be latched and the bridges will remain in high impedance state for the toff time.

14.3.4 Switch configuration

Each bridge can be configured to be used as 2 independent switches that connects the output to supply or to ground. It is also possible to parallel the two switches and use them as a single super switch.

All resulting switches will behave according to the following truth table.

Table 34. Switch truth

TSD	nReset	Low power mode	Enable	Current limit	MtrXCtrl SideA/B	PWM	OUT
1	X	X	X	X	X	X	Z
0	0	X	X	X	X	X	Z
0	1	1	X	X	X	X	Z
0	1	0	0	X	X	X	Z
0	1	0	1	0	0	X	Z
0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	1	1	X	X	Z

Note: When “Low Power mode” bit is active the bridge will reduce its biasing thus contributing to the whole power saving.

When a current limit event occurs this event will be latched and the bridge will remain in high impedance state for the toff time.

14.3.5 Bipolar stepper configuration

The bridges 3 and 4 can be configured to be used as a micro-stepping, bidirectional driver for bipolar stepper motors.

The primary features of the driver are the following:

– Internal PWM current control.
– Micro stepping.
– Fast, mixed and slow current decay modes.

Each H-bridge is controlled with a fixed and selectable off-time PWM current-control circuit that limits the load current to a value set by choosing $V_{STEPREF}$ voltage by means of the internal DAC and an the external R_{SENSE} value.

The max current level could be calculated using the formula:

$$I_{MAX}=V_{STEPREF}/R_{SENSE}$$

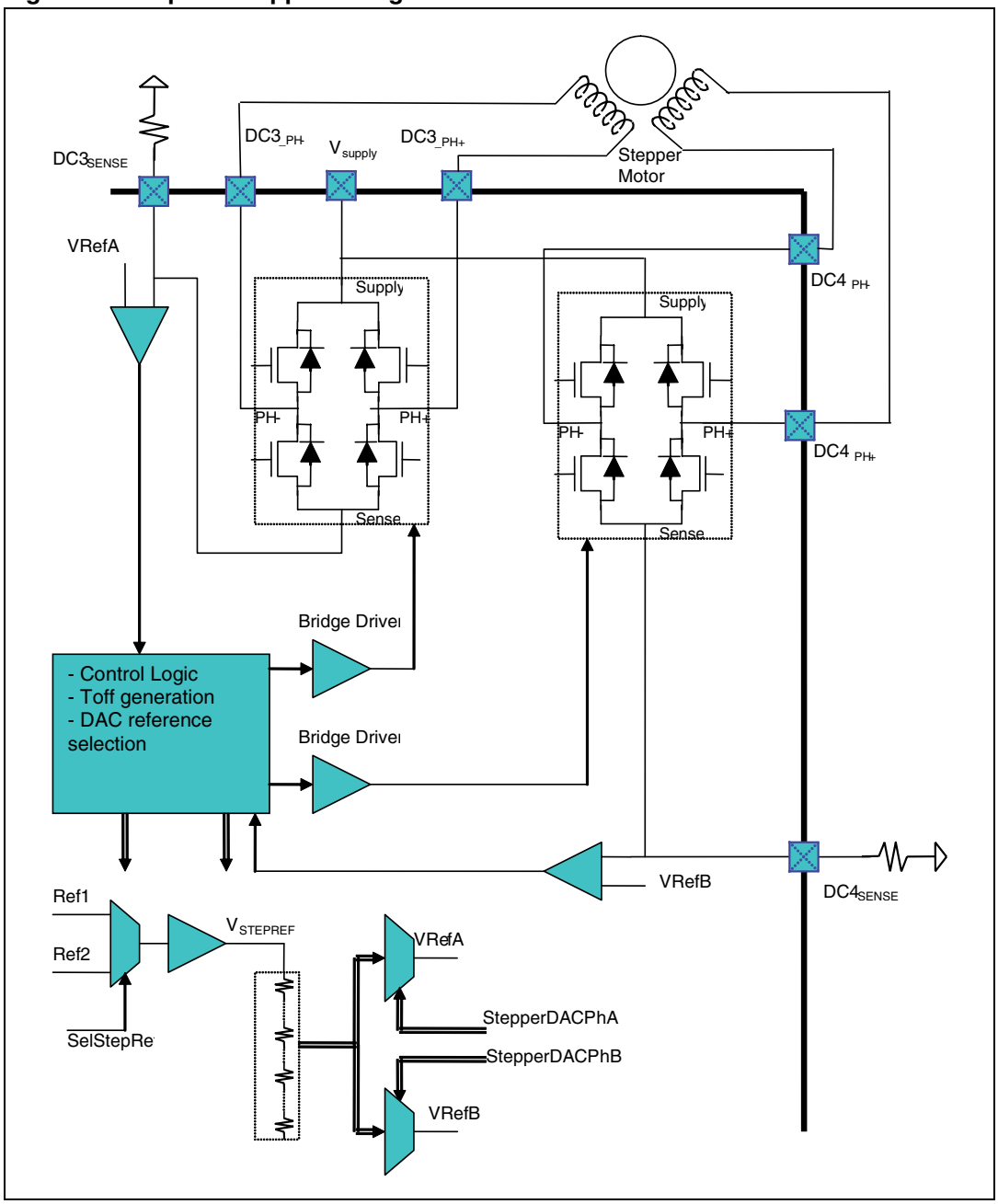
To obtain the best current profile, the user can choose three different current decay modes: slow, fast and mixed. Initially, during Ton, a diagonal pair of source and sink power MOS is enabled and current flows through the motor winding and the sense resistor. When the voltage across the sense resistor reaches the programmed DAC output voltage, the control logic will change the status of the bridge according to the selected decay mode (slow, fast or mixed). In slow decay mode the current is recirculated through the path including both high side power MOS for the whole toff time. In fast decay mode the current is recirculated through the high and low side power MOS opposite respect to those forcing current to

increase. Mixed decay mode is a selectable mix of the previous two modes (fast decay followed by slow decay) and allows the user to find the best trade off between load current ripple and fast current levels transition. Additionally, by setting the SeqMixedOnlyInDecreasingPh bit in the StpCfg1 register, the user can choose to apply the fast decay percentage in mixed mode always or only when the current is decreasing (i.e from 90° to 180° and from 270° to 360° of the sinusoidal wave).

By using SPI interface the user can choose:

- Control type (external firmware control, half step, normal drive, wave drive, micro-step).
- Up to 16 current levels (quasi-sinusoidal increments) for each bridge.
- Current direction.
- Decay mode.
- Blanking time.
- Off time (32 values from 2µs to 64µs).
- Percentage of fast decay respect to toff (when in mixed decay mode).

Figure 16. Bipolar stepper configuration



The operating characteristics remain the same (when applicable) already seen in the power bridges operating specifications with the addition of the following:

Table 35. Stepper specifications

Parameter	Description	Test condition	Min	Typ	Max	Unit
$V_{STEPREF}$	Reference voltage	SelStepRef =0 SelStepRef =1	0.480 0.720	0.50 0.75	0.520 0.780	V
Sense_off	Sense comparator offset		-12		12	mV

Using the StepCtrlMode[2:0] bits in StepCfg1 register, S.A.B.Re can be programmed to internally generate the stepping levels. In these cases and depending on the StepFromGpio bit in the StpCfg1 register the Stepper driver will move to next step each time the StepCmd bit is set at logic level “1” or at each pulse transition longer than ~1µs externally applied on GPIO12 (StepReq signal), according to following table:

Table 36. Sequencer drive

StepFromGpio	Sequencer driven by
0	StepCmd bit in StepCmd register.
1	GPIO12 input pin.

The allowable control modes are as follows:

1. Stepping sequence left to external microcontroller: in this mode the current level in each motor winding is set by the microcontroller via the serial interface.
2. Full step: in this mode the electrical angle will change by 90° steps at each StepReq signal transition. There are two possibilities:
   – Normal step (two phases on): in normal step mode both windings are energized simultaneously and the current will be alternately reversed. The resulting electrical angles will be 45°, 135°, 225° and 315°.
   – Wave drive (one phase on): In wave drive mode each winding is alternately energized and reversed. The resulting electrical angles will be 90°, 180° and 270° and 360°.
3. Half step: in this mode, one motor winding is energized and then two windings alternately so the electrical angles the motor will do when rotating in clockwise direction and using the same current limit in both the phases are: 45°, 90°, 135°, 180°, 225°, 270°, 315° and 360°.
4. Microstepping: in this mode the current in each motor winding has a quasi sinusoidal profile. The increment between each step is obtained at each transition of StepCmd bit in StepCmd register. The difference between each step could be chosen (4, 8 or 16 levels for each phase) according to following table:

Table 37. Stepper mode

StepCtrlMode[2:0]	Control mode	Description
000 or 111	No Control	Stepping sequence control left to the external controller
001	Half Step	Half step
010	Normal Step	Full step (two phases on)
011	Wave Drive	Full step (one phase on)
100	1/4 Step	Four micro steps
101	1/8 Step	Eight micro steps
110	1/16 Step	Sixteen micro steps

Note: When in 1/16 step mode, the best phase approximation of sinusoidal wave, is obtained by repeating the “F” step as follows: 0, 1, 2, 3, … , D, E, F, F, F, E, D, … , 3, 2, 1, 0

When internal stepping sequence generation is used, the stepping direction is set by the StepDir bit according to the following table.

Table 38. Stepper sequencer direction

StepDir	Direction
0	Counter Clockwise (CCW)
1	Clockwise (CW)

Note: It is intended as clockwise the sequence that forces a clockwise rotation of the versors representing the current module and phase.

An internal DAC is used to digitally control the output regulated current. The available values are chosen to provide a quasi sinusoidal profile of the current. The current limit in each phase is decided by PhADAC[3:0] bits for phase A and PhBDAC[3:0] bits for phase B. The table below describes the relation between the value programmed in the stepper DAC and the current level:

Table 39. DAC

PhXDAC [3:0]	Phase Current ratio respect to I_{MAX}			
	Min	Typ	Max	Unit
0000		(Hi-Z)		
0001	7.8	9.8	11.8	% of I_{MAX}
0010	17.5	19.5	21.5	% of I_{MAX}
0011	27.0	29.0	31.0	% of I_{MAX}
0100	36.3	38.3	40.3	% of I_{MAX}
0101	45.1	47.1	49.1	% of I_{MAX}
0110	53.6	55.6	57.6	% of I_{MAX}
0111	61.4	63.4	65.4	% of I_{MAX}
1000	68.7	70.7	72.7	% of I_{MAX}
1001	75.3	77.3	79.3	% of I_{MAX}
1010	81.1	83.1	85.1	% of I_{MAX}
1011	86.2	88.2	90.2	% of IMAX
1100	90.4	92.4	94.4	% of I_{MAX}
1101	93.7	95.7	97.7	% of I_{MAX}
1110	96.5	98.1	99.7	% of I_{MAX}
1111		I_{MAX}		

Note: The Min and Max values are guaranteed by testing the percentage of VSTEPREF that allows the commuatation of the Rsense comparator.

$I_{MAX}=V_{STEPREF}/ R_{SENSE}$.

To obtain the best phase approximation of a sinusoidal wave, the user needs to repeat the final (100%) value. So the full values sequence should be as follows: 0, 1, 2, 3 … D, E, F, F, F, E, D … 3, 2, 1, 0.

Even if the total spread shows overlapping between current steps, the monotonicity is guaranteed by design.

When the internal sequencer the minimum angle resolution is nominally 5.625°, so depending on the control mode chosen, the selectable steps are the following:

Table 40. Internal sequencer

Control mode						Typical output current (% of IMAX)		Resulting electrical angle
Half step	Full step (2 phases on)	Full step (1 phase on)	1/4 step	1/8 step	1/16 step	Phase A (sin)	Phase B (cos)	Electrical degrees
1	1		1	1	1	70.7	70.7	45°
					2	77.3	63.4	50.6°
				2	3	83.1	55.6	56.2°
					4	88.2	47.1	61.9°
			2	3	5	92.4	38.3	67.5°
					6	95.7	29.0	73.1°
				4	7	98.1	19.5	78.8°
					8	100	9.8	84.4°
2		1	3	5	9	100	HiZ	90°
					10	100	-9.8	95.6°
				6	11	98.1	-19.5	101.2°
					12	95.7	-29.0	106.9°
			4	7	13	92.4	-38.3	112.5°
					14	88.2	-47.1	118.1°
				8	15	83.1	-55.6	123.8°
					16	77.3	-63.4	129.4°
3	2		5	9	17	70.7	-70.7	135°
					18	63.4	-77.3	140.6°
				10	19	55.6	-83.1	146.2°
					20	47.1	-88.2	151.9°
			6	11	21	38.3	-92.4	157.5°
					22	29.0	-95.7	163.1°
				12	23	19.5	-98.1	168.8°
					24	9.8	-100	174.4°
4		2	7	13	25	HiZ	-100	180°
					26	-9.8	-100	185.6°
				14	27	-19.5	-98.1	191.2°
					28	-29.0	-95.7	196.9°

Table 40. Internal sequencer (continued)

Control mode						Typical output current (% of IMAX)		Resulting electrical angle
Half step	Full step (2 phases on)	Full step (1 phase on)	1/4 step	1/8 step	1/16 step	Phase A (sin)	Phase B (cos)	Electrical degrees
			8	15	29	-38.3	-92.4	202.5°
					30	-47.1	-88.2	208.1°
				16	31	-55.6	-83.1	213.8°
	3				32	-63.4	-77.3	219.4°
5			9	17	33	-70.7	-70.7	225°
					34	-77.3	-63.4	230.6°
				18	35	-83.1	-55.6	236.2°
					36	-88.2	-47.1	241.9°
			10	19	37	-92.4	-38.3	247.5°
					38	-95.7	-29.0	253.1°
				20	39	-98.1	-19.5	258.8°
					40	-100	-9.8	264.4°
6		3	11	21	41	-100	HiZ	270°
					42	-100	9.8	275.6°
				22	43	-98.1	19.5	281.2°
					44	-95.7	29.0	286.9°
			12	23	45	-92.4	38.3	292.5°
					46	-88.2	47.1	298.1°
				24	47	-83.1	55.6	303.8°
					48	-77.3	63.4	309.4°
7	4		13	25	49	-70.7	70.7	315°
					50	-63.4	77.3	320.6°
				26	51	-55.6	83.1	326.2°
					52	-47.1	88.2	331.9°
			14	27	53	-38.3	92.4	337.5°
					54	-29.0	95.7	343.1°
				28	55	-19.5	98.1	348.8°
					56	-9.8	100	354.4°
8		4	15	29	57	HiZ	100	360°/0°
					58	9.8	100	5.6°
				30	59	19.5	98.1	11.2°

Table 40. Internal sequencer (continued)

Control mode						Typical output current (% of IMAX)		Resulting electrical angle
Half step	Full step (2 phases on)	Full step (1 phase on)	1/4 step	1/8 step	1/16 step	Phase A (sin)	Phase B (cos)	Electrical degrees
					60	29.0	95.7	16.9°
			16	31	61	38.3	92.4	22.5°
					62	47.1	88.2	28.1°
				32	63	55.6	83.1	33.8°
					64	63.4	77.3	39.4°

The voltage spikes on Rsense could be filtered by selecting an appropriate blanking time on the output of Current sense comparator. The Blanking time selection is made by using the StepBlkTime[1:0] bits in the StpCfg1 register, according to following table:

Table 41. Blanking times specification

StepBlkTime[1]	StepBlkTime[0]	Blanking time			Unit	Comments
		Min	Typ	Max		
0	0	0.6	0.95	1.2	us	Default value
0	1	0.95	1.4	1.85	us	
1	0	1.5	2.25	3	us	
1	1	3	4.25	5.5	us	

The stepper driver toff time could be programmed by means of the StepOffTime[4:0] bits in StpCfg1 register:

Table 42. Stepper off time

StepOffTime[4:0]	Off time	Unit
	Typ	
00000	2	us
00001	4	us
00010	6	us
00011	8	us
00100	10	us
00101	12	us
00110	14	us
00111	16	us
01000	18	us

Table 42. Stepper off time (continued)

StepOffTime[4:0]	Off time	Unit
	Typ	
01001	20	us
01010	22	us
01011	24	us
01100	26	us
01101	28	us
01110	30	us
01111	32	us
10000	34	us
10001	36	us
10010	38	us
10011	40	us
10100	42	us
10101	44	us
10110	46	us
10111	48	us
11000	50	us
11001	52	us
11010	54	us
11011	56	us
11100	58	us
11101	60	us
11110	62	us
11111	64	us

By means of MixDecPhA[4:0] and MixDecPhB[4:0] in StepCfg2 register, the percentage of Toff time during which each phase will stay in fast decay mode could be programmed according to following table:

Table 43. Stepper fast decay

MixDecPhX[4:0]	Fast decay percentage during toff	Unit
	Typ	
00000	0	%
00001	6.25	%
00010	12.5	%
00011	18.75	%
00100	25	%
00101	31.25	%
00110	37.6	%
00111	43.75	%
01000	50	%
01001	56.25	%
01010	62.5	%
01011	68.75	%
01100	75	%
01101	81.25	%
01110	87.5	%
01111	93.75	%
1xxxx	100	%

14.3.6 Synchronous buck regulator configuration

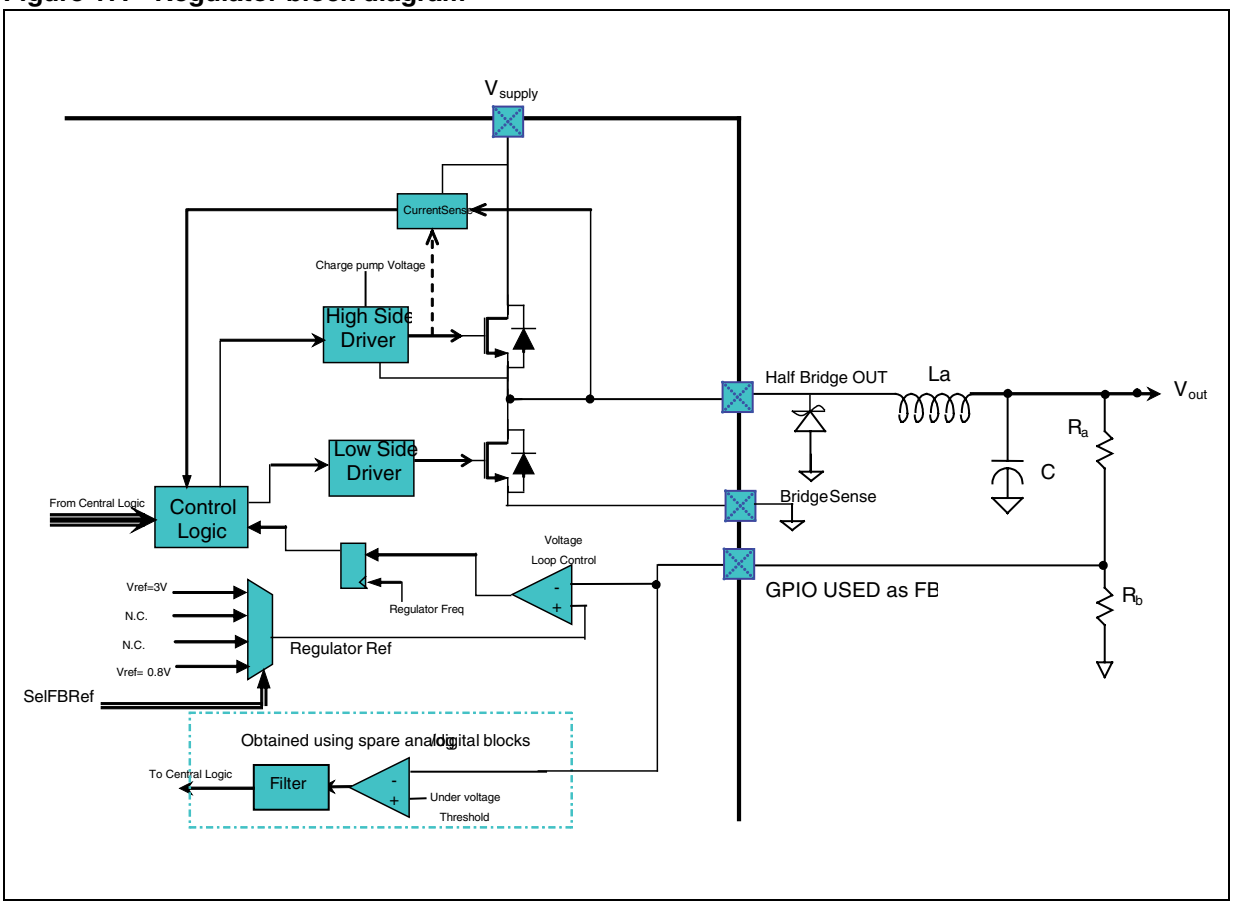
Bridge 3 can be configured to be used as 2 independent synchronous buck regulators or as a single high current synchronous buck regulator using GPIOs pins in order to close the voltage loop. The resulting regulator(s) will implement a non linear, pulse skipping, control loop using an internally generated PWM signal. The voltage will be set externally with a divider network and PWM duty cycle that can be programmed in order to ensure a proper regulation.

The regulator will be enabled/disabled using serial interface and will implement a soft start strategy similar to that used by primary switching regulator.

Here after are summarized the primary features of the regulator(s):

- Synchronous rectification
- Automatic low side disabling when current in the inductance reaches 0 to optimize efficiency at low load
- Pulse skipping control
- Internally generated PWM
- Cycle by cycle current limiting using internal current sensor
- Protected against load short circuit
- Soft start circuitry
- Under voltage signal (both continuous and latched) accessible through serial interface.

Figure 17. Regulator block diagram



Depending on the load current, there could be the necessity to add a Schottky diode on output to reduce internal thermal dissipation. This diode must be placed near to the pin and must be fast recovery and low series resistance type.

For detail about pulse skipping please refer to main switching regulator paragraph.

The output voltage will be externally set by a divider network connected on feedback pin. To reduce as much as possible the regulation voltage error S.A.B.Re has the possibility to switch between four regulator feedback voltage references (and, as a consequence, four under-voltage thresholds) using serial interface. The feedback reference voltage is selected

by writing the SelFBRef[1:0] bits in the Aux1SwCfg or Aux2SwCfg registers according to the following table:

Table 44. Switching regulator controller PWM specification

SelFBRef[1:0]		Reference voltage (V_{FBREF})				Comments
SelFBref[1]	SelFBref[0]	Min	Typ	Max	Unit	
0	0	0.776	0.8	0.824	V	
0	1	0.970	1	1.030	V	Default voltage for AUX1
1	0	2.425	2.5	2.575	V	Default voltage for AUX2
1	1	2.910	3	3.09	V	

The switching regulators have four possible PWM duty cycles that can be changed using SPI according to following table:

Table 45. Pwm specification

AuxXPWMTable[1:0]	Typical duty cycle value	Comments
00	10%	
01	13%	Default state for AUX1
10	24%	Default state for AUX2
11	61%	

The operating characteristics remain the same (when applicable) already seen in the *Section 15.2* with the addition of the following:

Table 46. Operating specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{AUX_SW}	Output pin voltage range	(1)	-1		V_{Supply}	V
I_Q	Output leakage current	$T_{junction}$ = 125°C	-50		+50	µA
I_{Qlp}	Output leakage current in “Low Power Mode”	V_{Supply} = 36V $T_{junction}$ = 125°C	-10		+10	µA
I_{Qfb}	GPIO feedback pin current	$T_{junction}$ = 125°C 0V≤Feedback ≤ 3V	-10		+10	µA
V^{out}	Output voltage range	V_{Supply} = 36V(2)	0.8		30	V
I_{load}	Output load current	V_{Supply} = 36V	0.002		1.5	A
R_{onH}	Internal high/low side RDSon	$T_{junction}$ = 125°C Iload=1A			0.8	Ω
V_{loop}	Loop voltage accuracy			±3%		
V_{regR}	Output voltage ripple (RMS)	L = TBD, C = TBD/ESR=TBD mΩ(3)		TBD		mV_{RMS}
V_{uvFall}	Under voltage falling threshold	(4)	84.5	87	89.5	%
V_{uvRise}	Under voltage rising threshold	(4)	90.5	93	95.5	%

Table 46. Operating specification (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{uvhys}	Under voltage hysteresis			6		%
t_{aux_uv}	Under voltage deglitch filter			5		µs
I_{limit}	Current limit protection		1.6		2.5	A
$t_{deglitch}$	Current limit deglitch time		50			ns
t_{I_lim}	Current limit response time	In normal operating mode (no UV)(5)			700	ns
t_{I_limUV}	Current limit response time in UV condition.	When in Under Voltage(6)			500	ns
t_r	Switching output rise time	V_{Supply} = 36V, Resistive load to gnd: R=422 Ω(7)	5		30	ns
t_f	Switching output fall time	V_{Supply} = 36V, Resistive load to gnd = 10 Ω(7)	10		50	ns
t_{dead}	Crossover dead time			100		ns
F_{regPwm}	Operating frequency			Fosc/64		kHz

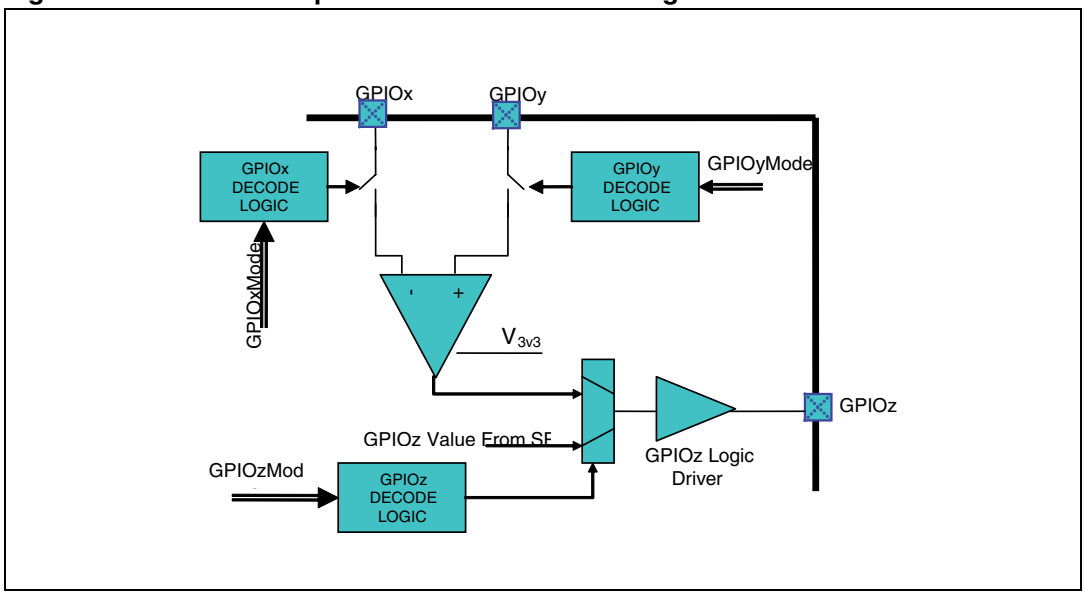
1. The external components connected to the pin must be chosen to avoid that the voltage exceeds this operative range.
2. The regulated voltage can be calculated using the formula: VMAIN_SW = VFBREF *(Ra+Rb)/Rb.
3. The choice of proper values for L and C depends from the application.
4. Undervoltage rising and falling thresholds are intended as a percentage of feedback pin voltage (VSW_main_FB).
5. This condition is intended to simulate an extra current on output.
6. This condition is intended to simulate a short circuit on output.
7. Rise time is measured between 10% and 90% of supply voltage.

14.3.7 Regulation loop

As seen before S.A.B.Re contains 2 regulation loops for switching regulators that are used when bridge 3 is used as a regulator. These loops are assembled using internal comparators and filters similar to that used in main switching regulator.

When bridge 3 is not used for this purpose or when only one regulation loop is needed, the control loop is available on a GPIO output thus enabling the customer to assembly a basic buck switching regulator using an external Power FET. The comparators used in the above mentioned regulation loops are general purpose low voltage (3.3 V) comparators; when the relative regulation loop is not used they can be accessed as shown in the diagram here below:

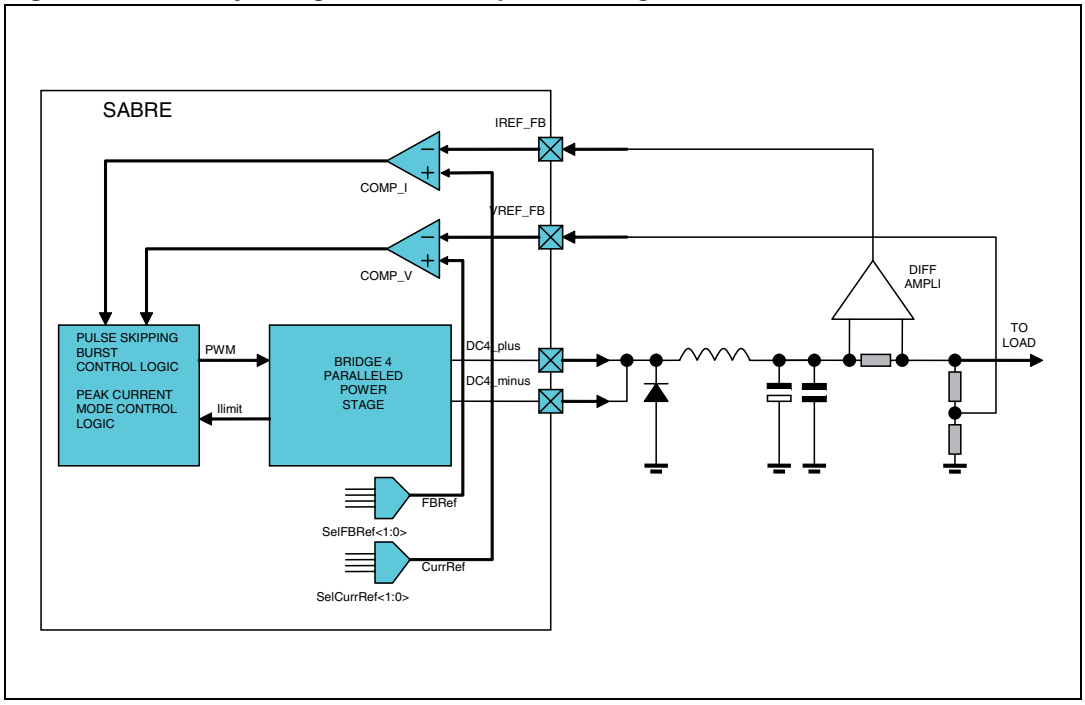
Figure 18. Internal comparator functional block diagram



The functionality of this circuit is obtained by using the bridge 4 output stage. This circuit is powered directly from V_{Supply} and it is intended to be used as a battery charger or a switching regulator.

The control loop block diagram is shown in the following figure:

Figure 19. Battery charger control loop block diagram



The battery charger control loop implements an asynchronous switching regulator intended to be used as a constant voltage/constant current programmable source.

When used as a simple switching regulator, it could be a system regulator depending on startup configurations

When a system regulator under-voltage event is detected S.A.B.Re will enter in reset state signaling this event to the microcontroller by pulling low the nRESET pin and disabling most of its internal blocks.

Battery charger regulator application (CC-CV).

When the control loop is intended to be used as a battery charger, the Aux3BatteryCharge bit must be written in the Aux3SwCfg1 register. This is because in this case the undervoltage event that will be sure present when charging a battery (see next battery charger profile) will not be considered during start up sequence.

Voltage regulation

The regulated output voltage will be externally set by a resistor divider network connected to VREF_FB pin. S.A.B.Re has the possibility to choose between four voltage references (and, as a consequence, four under-voltage thresholds) using the serial interface. The feedback reference voltage selection is made by writing the SelFBRef[1:0] bits in the Aux3SwCfg1 register according to the table here below:

Table 47. Battery charger control loop FBRef specification

Aux3SwCfg1		Reference voltage (FBRef)				Comments
SelFBref[1]	SelFBref[0]	Min	Typ	Max	Unit	
0	0	1.370	1.412	1.455	V	
0	1	1.746	1.8	1.854	V	Default state
1	0	2.079	2.143	2.207	V	
1	1	2.425	2.5	2.575	V	

Reference voltages values can be changed using a metal layer change in order to adapt them to customer system.

The first, second and third reference voltage has been chosen to regulate 3.3V, 4.2V and 5V with the same resistor divider network, such that the commutation between different regulated voltages can be done on the fly in the application.

Current regulation

The regulation of the output current can be done externally, by using a sense resistor connected in series on the path that provides current to the load. By using an external differential amplifier the customer can set the desired V=f(I) characteristic, and therefore the regulated current: the voltage provided at the I_{REF_FB} pin will be compared to the internal reference. S.A.B.Re has the possibility to choose between four voltage references using the serial interface, writing the SelCurrRef[1:0] bits in the Aux3SwCfg1 register according to the following the table:

Table 48. Battery charger control loop CurrRef specification

Aux3SwCfg1		Reference voltage (CurrRef)				Comments
SelCurrRef[1]	SelCurrRef[0]	Min	Typ	Max	Unit	
0	0	0.873	0.900	0.927	V	Default state
0	1	1.394	1.437	1.480	V	
1	0	1.746	1.8	1.854	V	
1	1	2.182	2.25	2.318	V	

Adjustable reference voltages values can be changed using a metal layer change in order to adapt them to customer system.

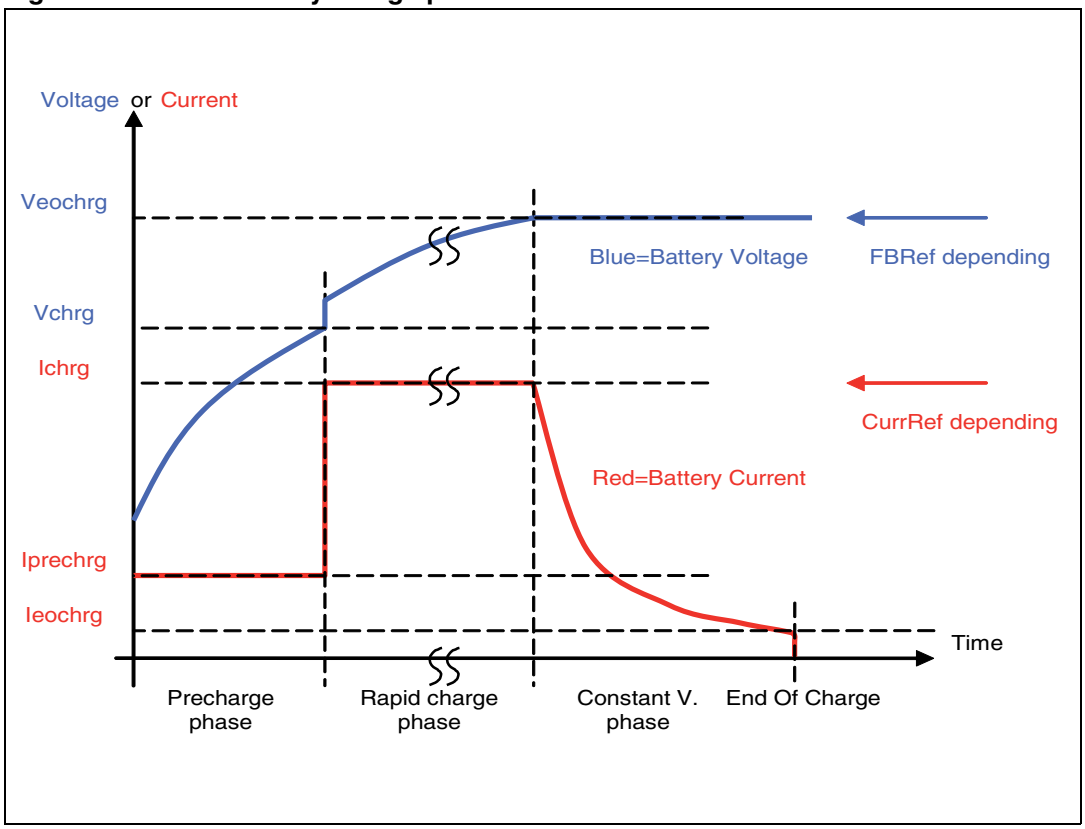
Regardless of the CurrRef voltage, if the I_{REF_FB} pin remains below the chosen threshold, the internal current limitation will work (see DC motor paragraph, Bridge4 Ilimit).

Battery charge profile

The battery charge profile can be chosen by fixing the desired CurrRef and FBRef internal reference voltages and by choosing the desired V=f(I) trans-characteristic of the external differential amplifier.

The following is a typical Li-Ion battery charge profile:

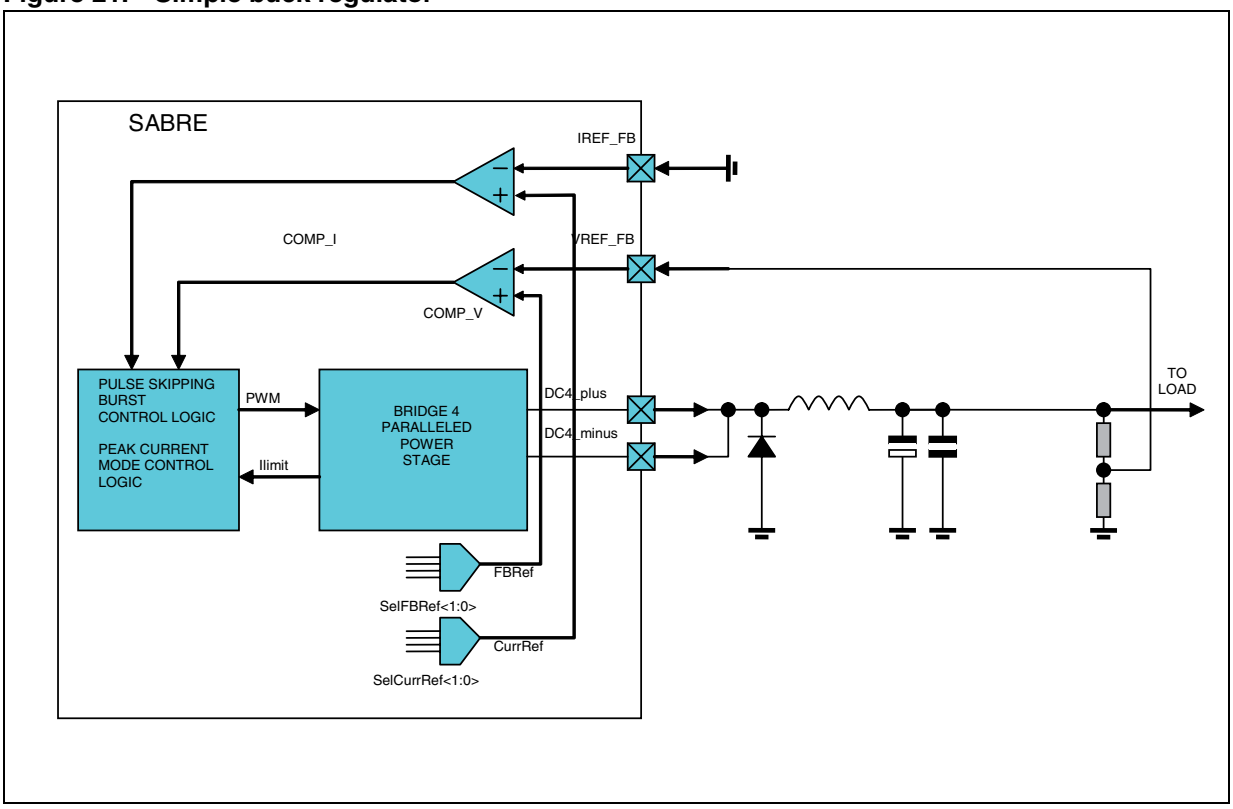
Figure 20. Li-ion battery charge profile



Simple buck regulator application

The battery charge loop control can be used to implement a buck type switching regulator. The regulated output voltage will be externally set by a resistor divider network connected to V_{REF_FB} pin, as already described in voltage regulation section, and the current protection will be the one implemented internally in the Bridge4 section.

Figure 21. Simple buck regulator



When this control loop is intended to be used as a simple buck regulator, the proper Aux3BatteryCharge bit must be written in the Aux3SwCfg1 register.

The regulator will also implement a soft start strategy.

When S.A.B.Re “Low Power mode” is enabled this regulator will be disabled.

Here after are summarized the primary features of the regulator:

- Internal power switch.
- Nonlinear pulse skipping control.
- Internally generated PWM (250 KHz switching frequency).
- Cycle by cycle current limiting using internal current sensor/ external current sense differential amplifier.
- Protected against load short circuit.
- Soft start circuitry to limit inrush current flow from primary supply.
- Under voltage signal (both continuous and latched) accessible through SPI.
- Over temperature protection.

In pulse skipping control PWM the duty cycle must be decided by the user depending on supply voltage and regulated voltage.

Therefore the switching regulator has 4 possible PWM duty cycles that can be changed writing in the Aux3PWMTable[1:0] bits in the Aux3SwCfg1 register according to the following table.

Table 49. Battery charger regulator controller PWM specification

Aux3PWMTable [1:0]	Typical duty cycle value	Comments
00	10%	
01	13%	
10	24%	Default state
11	61%	

Adjustable duty cycles can be changed using a metal layer change in order to adapt it to customer system. The only limitation is that ALL regulators share the same duty cycle bus, so any modification must consider ALL regulators needed duty cycles.

AUX3 Control loop parameters specifications

The following table assumes that DC4_PLUS and DC4_MINUS pins are externally shorted together.

Table 50. Battery charger operating specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{AUX_SW}	Output pin voltage range	(1)	-1		V_{Supply}	V
I_Q	Output leakage current	$T_{junction}$ = 125°C	-100		+100	µA
I_{Qlp}	Output leakage current in “Low Power Mode”	V_{Supply} = 36V $T_{junction}$ = 125°C	-20		+20	µA
I_{Qfb}	GPIo feedback pin current	$T_{junction}$ = 125°C 0V=Feedback=3V	-10		+10	µA
V_{out}	Output voltage range	V_{Supply} = 36V(2)	1.412		30	V
I_{load}	Output load current	V_{Supply} = 36V	0.002		3	A
R_{onH}	Internal high/low side RDson	$T_{junction}$ = 125°C Iload=1.5A			0.4	Ω
V_{loop}	Loop voltage accuracy			±3%		
V_{regR}	Output voltage ripple (RMS)	L = TBD, C = TBD,ESR=TBD mΩ(3)		TBD		mV_{RMS}
V_{uvFall}	Under voltage falling threshold	(4)	84.5	87	89.5	%
V_{uvRise}	Under voltage rising threshold	(4)	90.5	93	95.5	%

Table 50. Battery charger operating specification (continued)

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{uvhys}	Under voltage hysteresis			6		%
t_{aux_uv}	Under voltage deglitch filter			5		µs
I_{limit}	Current limit protection		3.1		5.3	A
$t_{deglitch}$	Current limit deglitch time		50			ns
t_{I_lim}	Current limit response time	In normal operating mode (no UV)(5)			700	ns
t_{I_limUV}	Current limit response time in UV condition.	When in Under Voltage(6)			500	ns
t_r	Switching output rise time	V_{Supply} = 36V, Resistive load to gnd = 422 Ω(7)	5		30	ns
t_f	Switching output fall time	V_{Supply} = 36V, Resistive load to gnd = 10 Ω(6)	10		50	ns
t_{dead}	Crossover dead time			100		ns
F_{regPwm}	Operating frequency			Fosc/64		kHz

1. The external components connected to the pin must be chosen to avoid that the voltage exceeds this operative range.
2. The regulated voltage can be calculated using the formula: VMAIN_SW = VFBREF *(Ra+Rb)/Rb.
3. The choice of proper values for L and C depends from the application.
4. Undervoltage rising and falling thresholds are intended as a percentage of feedback pin voltage (VSW_main_FB).
5. This condition is intended to simulate an extra current on output.
6. This condition is intended to simulate a short circuit on output.
7. Rise time is measured between 10% and 90% of supply voltage.

15 AD converter

15.1 Overview

S.A.B.Re integrates and makes accessible via SPI a general purpose multi-input channel 3.3V analog to digital converter (ADC).

The ADC can be configured to be used as:

- 8-bit resolution ADC.
- 9-bit resolution ADC.

The result of the conversion will always be a 9-bit word; the difference between the two configurations is that, to speed up the conversion, the resolution is reduced when the ADC is used in the 8-bit resolution mode.

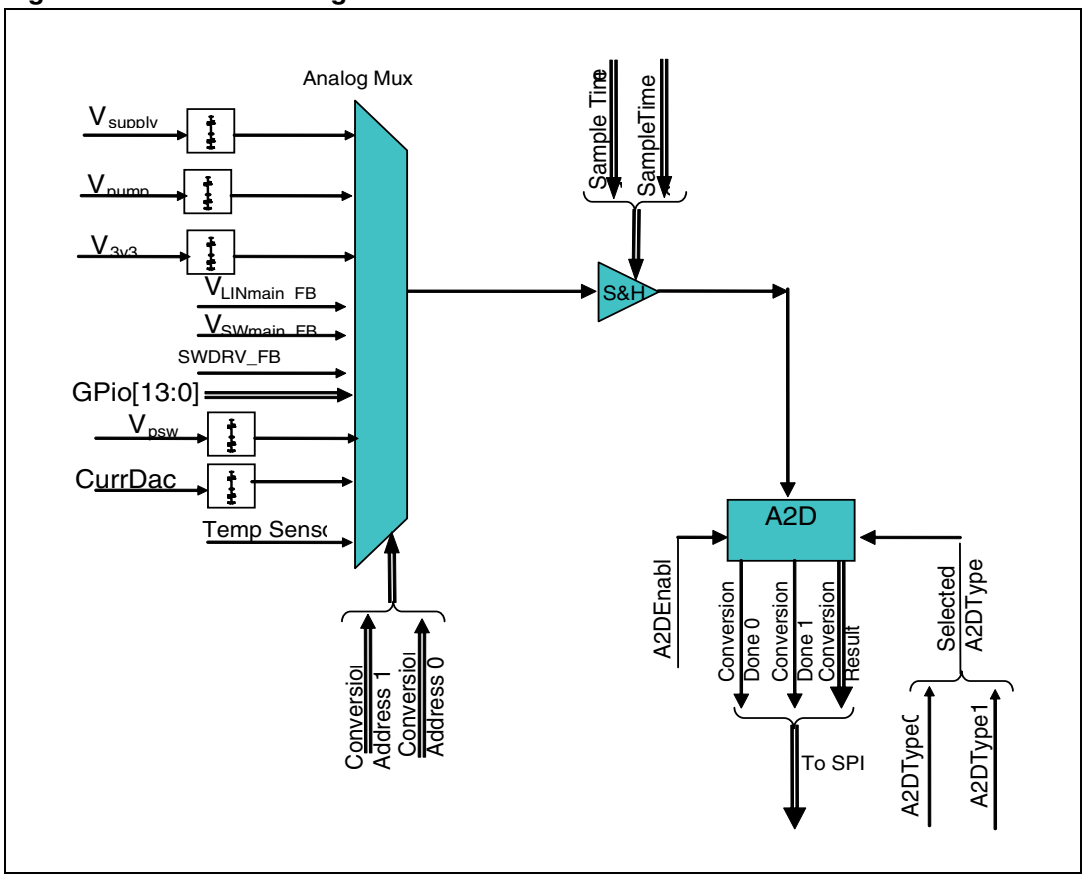
The ADC is seen at software level as a 2 channel ADC with different programmable sample times; a finite state machine will sample the requests done through the SPI interface on both the channel and will execute them in sequence.

When used as 8-bit resolution the ADC can achieve a higher throughput and, if the minimum sample time is used, one conversion is completed in t = 5.5µs. When used as 9-bit resolution ADC the circuit is slower and the minimum sample times are disabled. In that case the conversion will be completed in a time t= 10 µs

The use of ADC type must be decided at the start-up by writing in the one time programmable ADC configuration register; no A/D conversion will be enabled if this register is not set from last power-up sequence.

This ADC can be used to measure some external pins as well as some S.A.B.Re's internal voltages. The converter is based on a cyclic architecture with an internal sample-and-hold circuit. Sample time can be changed using serial interface to enable good measure of higher impedance sources.

Figure 22. A2D block diagram



The A2D system is enabled by setting the A2DEnable bit to '1' in the A2DControl register.

The A2DType bit in the A2DConfigX registers selects the A2D active configuration (8-bit resolution or 9-bit) according to the following truth table:

Table 51. ADC truth

A2DEnable	A2DType0/1	A2D operation
0	X	Disabled
1	0	ADC working as a 8-bit ADC
1	1	ADC working as a 9-bit ADC

The multiplexer channel to be converted can be chosen by writing the A2DChannel1[4:0] or A2DChannel2[4:0] bits in the A2DConfigX register; the channel addresses table is reported in the following table.

Table 52. Channel addresses

A2DChannelX[4:0] (bin.)	Converted channel	Note
00000	V_{Supply} scaled	See voltage divider specification.
00001	$V_{SupplyInt}$ scaled	See voltage divider specification.
00010	$V_{ref\_2\_5V}$	
00011	Temp Sensor1	Temperature sensor1
00100	Temp Sensor2	Temperature sensor2
00101	V_{3v3} scaled	See voltage divider specification.
0011X	Not used	
01000	Not used	
01001	GPIO[0]	
01010	GPIO[1]	
01011	GPIO[2]	
01100	GPIO[3]	
01101	GPIO[4]	
01110	GPIO[5]	
01111	GPIO[6]	
10000	GPIO[7]	
10001	GPIO[8] clamp	See current DAC circuit
10010	GPIO[9]	
10011	GPIO[10]	
10100	GPIO[11]	
10101	GPIO[12]	
10110	GPIO[13]	
10111	GPIO[14]	
11000	MuxRefOpAmp1	
11001	MuxRefOpAmp2	
11010	OutStripStepperPhA	
11011	OutStripStepperPhB	
11100	Not used	
11101	ST reserved	References AUX1 switching reg.
11110	ST reserved	0.8V reference voltage
11111	ST reserved	1.65V reference voltage

The sample time can be changed by modifying the A2DSampleX[2:0] bits in the A2DConfigX register; depending on which is the A2DType bit, the available sample times are reported in the following tables.

Table 53. ADC sample times when working as a 8-bit ADC

A2DSampleX[2:0] (binary)	Sample time	
	Typ	Unit
000	16*Tosc	µs
001	32*Tosc	µs
010	64*Tosc	µs
011	128*Tosc	µs
100	256*Tosc	µs
101	512*Tosc	µs
110	1024*Tosc	µs
111	2048*Tosc	µs

Table 54. ADC sample time when working as a 9-bit ADC

A2DSampleX[2:0] (binary)	Sample time	
	Typ	Unit
000	32*Tosc	µs
001	64*Tosc	µs
010	128*Tosc	µs
011	256*Tosc	µs
100	512*Tosc	µs
101	1024*Tosc	µs
110	2048*Tosc	µs
111	4096*Tosc	µs

A conversion on channel 1 can be triggered by writing a logic ‘1’ in the A2DTrig1 bit in the A2DConfigX register and a conversion on channel 2 can be triggered writing a logic ‘1’ in the A2DTrig2 bit in the same register. While a request on a channel is pending but not yet completed S.A.B.Re will force to logic ‘0’ the corresponding A2DdoneX bit in the A2DResultX registers and S.A.B.Re will not accept other conversion request on that channel.

Continuous conversion on one channel can be accomplished by setting to logic ‘1’ the A2DcontinuousX bit in the A2DConfigX register. When A2DcontinuousX bit is set, other conversions can be accomplished on the other channel; these conversions will be inserted between two conversions of the other channel and the end of the conversion will be signaled using A2DdoneX bit. Of course when a channel is in continuous mode its sample time and channel address cannot be changed.

Continuous conversions on both 2 channels can be also accomplished by setting to logic ‘1’ the A2Dcontinuous1 and A2Dcontinuous2 bits; the conversions are made in sequence.

15.2 A2D specification with A2dType=0

Table 55. ADC specification

Parameter	Description	Test condition	Min	Typ	Max	Unit(1)
IMR	Measurement range	A2dType = 0	0		V_{3v3}	V
INL	Integral non-linearity	A2dType = 0(2)(3)			±1	LSB
DNL	Differential non-linearity	A2dType = 0(4)(3)			±1	LSB
OE	Offset error	A2dType = 0(5)			±4	LSB
OE_{Drift}	Offset error drift	A2dType = 0 over time and temperature			±3	LSB
GE	Gain error	A2dType = 0(6)			±4	LSB
GE_{Drift}	Gain error drift	A2dType = 0 over time and temperature			±4	LSB
t_{conv}	Minimum conversion time				5.5	µs
	Resolution	(7)	8			bits
Cin	Input capacitance	(8)			4	pF

1. The definition of LSB for this table is LSB=IMRmax/($2^{7.5}$-1).
2. Integral Non Linearity error (INL) is defined as the maximum distance between any point of the ADC characteristic and the “best straight line” approximating the ADC transfer curve.
3. The ADC ensures monotonic characteristic and no missing codes.
4. Differential nonlinearity error (DNL) is defined as the difference between an actual step width and the ideal width value of 1 LSB.
5. Offset error (OE) is the deviation of the first code transition (000...000 to 000...001) from the ideal (i.e. GND + 0.5 LSB).
6. Gain error (GE) is the deviation of the last code transition (111...110 to 111...111) from the ideal (V3v3 - 0.5 LSB), after adjusting for offset error.
7. Please note that the result of the conversion will always be a 9-bit word: to speed up the conversion, the resolution is reduced when the ADC is used in the 8- bit resolution mode.
8. Actual input capacitance depends on the pin that must be converted.

15.3 A2D specification with A2dType=1

Table 56. ADC specification

Parameter	Description	Test condition	Min	Typ	Max	Unit(1)
IMR	Measurement range	A2dType = 1	0		V_{3v3}	V
INL	Integral non-linearity	A2dType = 1(2)(3)			±1	LSB
DNL	Differential Non-Linearity	A2dType = 1(4)(3)			±1	LSB
OE	Offset error	A2dType = 1(5)			±4	LSB
OE_{Drift}	Offset error drift	A2dType = 1 over time and temperature			±3	LSB
GE	Gain error	A2dType = 1(6)			±4	LSB
GE_{Drift}	Gain error drift	A2dType = 1 over time and temperature			±4	LSB
t_{conv}	Minimum conversion time				10	µs
	Resolution		9			bits
Cin	Input capacitance	(7)			4	pF

1. The definition of LSB for this table is LSB=IMRmax/(2^9-1).
2. Integral non linearity error (INL) is defined as the maximum distance between any point of the ADC characteristic and the “best straight line” approximating the ADC transfer curve.
3. The ADC ensures monotonic characteristic and no missing codes.
4. Differential nonlinearity error (DNL) is defined as the difference between an actual step width and the ideal width value of 1 LSB.
5. Offset error (OE) is the deviation of the first code transition (000...000 to 000...001) from the ideal (i.e. GND + 0.5 LSB).
6. Gain error (GE) is the deviation of the last code transition (111...110 to 111...111) from the ideal (V3v3 - 0.5 LSB), after adjusting for offset error.
7. Actual input capacitance depends on the pin that must be converted.

15.4 Voltage divider specifications

As can be seen in the A2D block diagram, in order to report some voltages in the A2D working range, they are scaled with a resistor divider before the conversion.

Here below are reported the resistor voltage divider specifications:

Table 57. Voltage divider specification

Parameter	Description	Notes	Min	Typ	Max	Unit
R_{Supply_ratio}	V_{Supply} divider ratio		-10%	1/15	+10%	
$R_{SupplyInt\_ratio}$	$V_{Supply\ Int}$ divider ratio		-10%	1/15	+10%	
R_{v3v3_ratio}	V_{3v3} divider ratio		-10%	1/2	-10%	

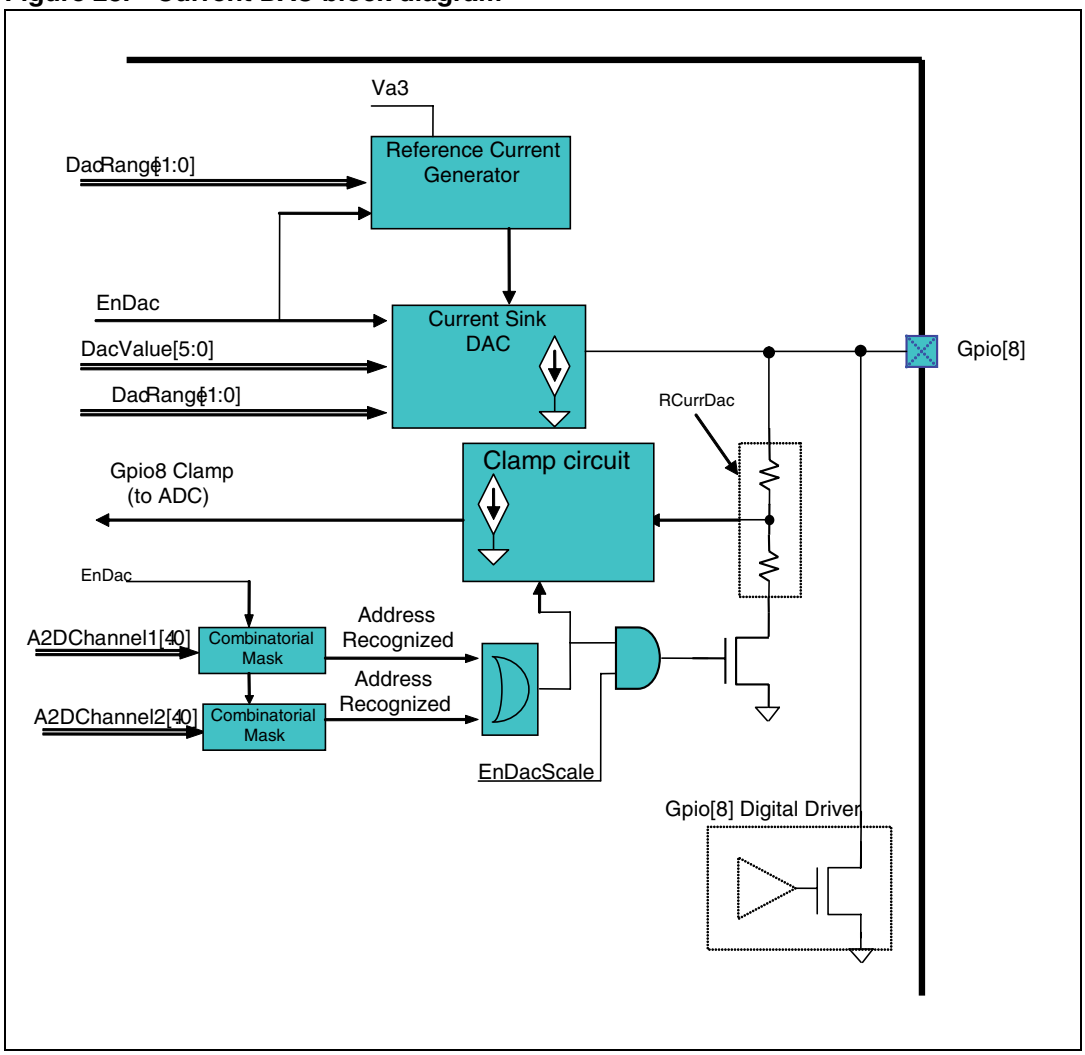
16 Current DAC circuit

16.1 Overview

S.A.B.Re includes a multiple range 6-bit current sink DAC. The LSB value of this DAC can be selected using the DacRange[1:0] bits in the CurrDacCtrl register.

The output of this circuit is connected to GPIO[8] that is a 5V tolerant pin. The value of this pin can be converted using ADC. The pin value can be scaled before being converted by enabling the internal resistor divider connected to this pin. If the current sunk by resistor divider is not acceptable the pin voltage can be converted without scaling its value. When the conversion without scaling resistor is chosen a clamping connection is used to avoid voltage compatibility of the pin to the ADC system. The clamping circuit will sink a typical current of half microampere from the pin during the sampling time.

Figure 23. Current DAC block diagram



The circuit is enabled by setting to logic ‘1’ the EnDac bit in the CurrDacCtrl register then the desired sunk current value is chosen by changing the value of the DacValue[5:0] bits in the

same register being DacValue[0] the least significant bit and DacValue[5] the most significant bit.

The current DAC has three possible current ranges that can be selected using the DacRange[1:0] bits in the CurrDacCtrl register . The DAC range selection table is shown here below:

Table 58. Current DAC truth

DacRange[1]	DacRange[0]	LSB typical current I_{LSB} typ	Full scale typical current I_{FULL} typ
0	0	Disabled	Disabled
0	1	10 µA	0.63 mA
1	0	100 µA	6.3 mA
1	1	1 mA	63 mA

By changing LSB current value, all steps will change following this relation:

$$I_{step}(N) = N * I_{LSB}$$

where N is the value of DacValue[5:0] bits.

Table 59. Current DAC specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_R	Pin voltage operative range	(1)	0.7		5.5	V
I_{OUT_OFF}	Output off leakage current	DacValue[5:0] = 000000	-1		+1	µA
$I_{FULL\_ERR\_01}$	Full scale current error	DacRange[1:0] =01 DacValue[5:0] = 111111	-10		10	% of $I_{FULL\ typ}$
$I_{FULL\_ERR\_10}$	Full scale current error	DacRange[1:0] =10 DacValue[5:0] = 111111	-13		13	% of $I_{FULL\ typ}$
$I_{FULL\_ERR\_11}$	Full scale current error	DacRange[1:0] =11 DacValue[5:0] = 111111	-12		12	% of $I_{FULL\ typ}$
INL_{10_11}	Integral non-linearity for 10 and 11 ranges				±2	LSB
DNL_{10_11}	Differential non-linearity for 10 and 11 ranges				±2	LSB
INL_{01}	Integral non-linearity for 01 range				±1	LSB
DNL_{01}	Differential non-linearity for 01 range				±1	LSB
$R_{CurrDac\_res}$	Gpio[8] divider total resistance		-25%	45	+25%	kΩ
$R_{CurrDac\_ratio}$	Gpio[8] divider ratio		-2.5%	3/5	+2.5%	
t_{set}	Settling time	(2)			5	µs

1. All parameters are guaranteed in the range between V_{OL} and $V_{R\ Max}$.
2. Measured from DacValue[5:0] change in SPI interface.

17 Operational amplifiers

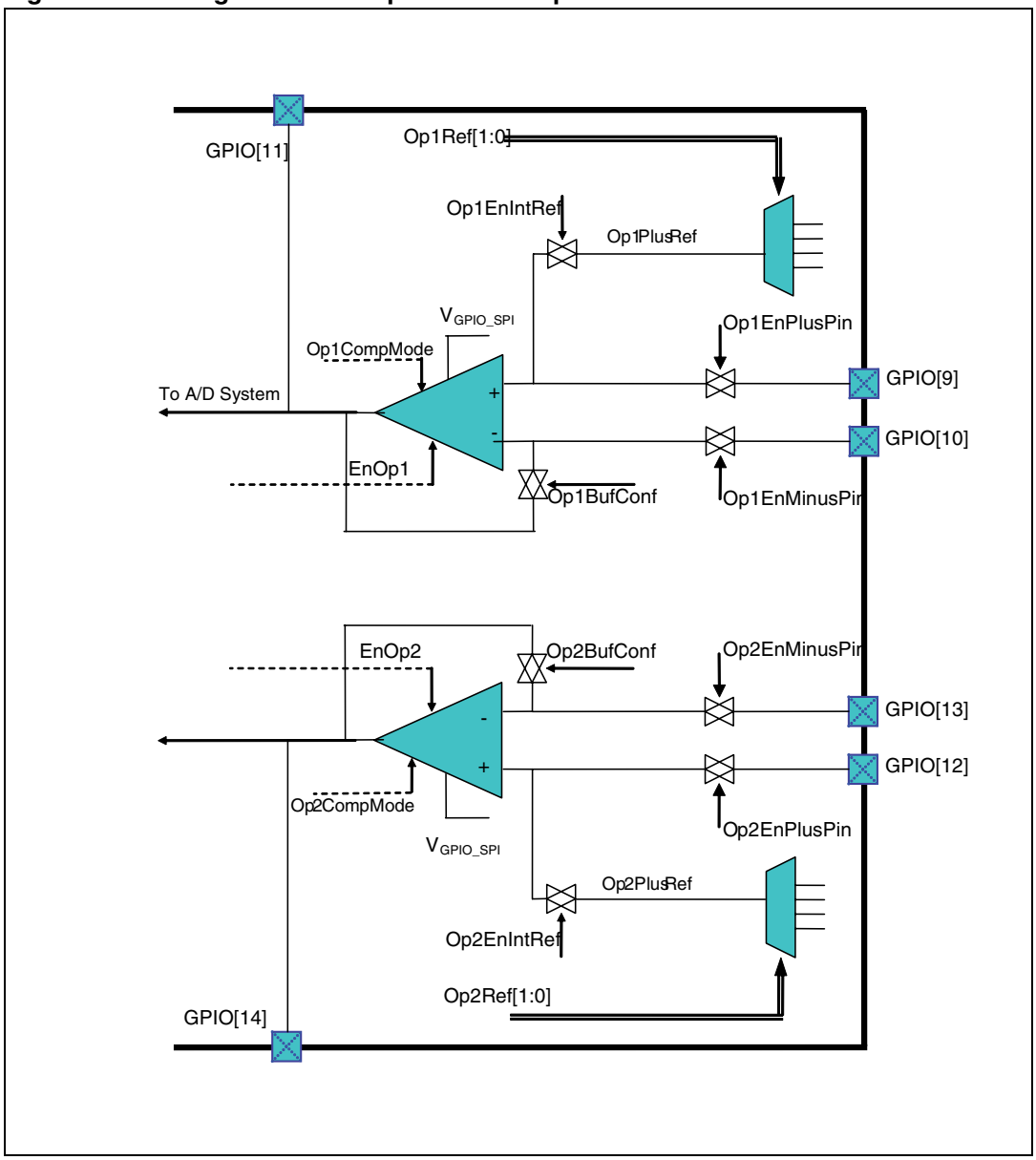
17.1 Overview

S.A.B.Re contains two rail to rail output, high bandwidth internally compensated operational amplifiers supplied by V_{GPIO_SPI} pin. The operative supply range is 3.3V±4.5%

Each operational amplifier can have all pin accessible or, to save pins, can be internally configured as a buffer. They can also be used as comparators; to do that the user must disable internal compensation by writing a logic level “1” in the OpXCompMode bit in the OpAmpXCtrl register.

Here below are reported the block diagrams of the two operational amplifiers

Figure 24. Configurable 3.3V operational amplifiers



Note: Op1EnPlusRef and Op2EnPlusRef cannot be used to drive external pin so the user must be sure not to enable the path between one of these voltage references and the external pin.

The operational amplifiers are capable to drive a capacitive load in buffer configuration up to a maximum of 100pF; for higher capacitance it is necessary to add resistive loads to increase the OP output current, and/or to add a low resistor (10 Ohm) in series to the load capacitance.

The table here below describes the main operational amplifier parameters.

17.2 Operational amplifiers specifications

Table 60. Configurable 3.3V operational amplifier specification
(Note: V_{GPIO_SPI}=3.3V unless otherwise specified)

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{GPIO_SPI}	Supply voltage range		3.15		3.45	V
V_{ICM}	Input common mode voltage range		0		V_{GPIO_SPI}	V
V_{OUT_MAX}	Output voltage	Iload =± 1mA	0.1		3.2	V
$V_{Op1PlusRef}$	Operational amplifier 1 reference voltage	Op1Ref[1:0]=00 Op1Ref[1:0]=01 Op1Ref[1:0]=10 Op1Ref[1:0]=11	0.970 1.600 1.940 2.425	1 1.65 2 2.5	1.030 1.700 2.060 2.575	V
$V_{Op1PlusRef}$	Operational amplifier 2 reference voltage	Op2Ref[1:0]=00 Op2Ref[1:0]=01 Op2Ref[1:0]=10 Op2Ref[1:0]=11	0.970 1.600 1.940 2.425	1 1.65 2 2.05	1.030 1.700 2.060 2.575	V
	Open loop gain	V_{ICM}=1.65V Il_{oad}= 0mA	90			dB
CMRR	Common mode rejection ratio			105		dB
	PSRR	Il_{oad}= ±6mA V_{ICM}=1.65V(1)		90		dB
I_{in_offs}	Input offset current				150	nA
I_{in_bias}	Input bias current				500	nA
V_{in_offs}	Input offset voltage		-5		5	mV
GBWP	Gain bandwidth product	Cload=100pF V_{ICM}=1.65V Rload=330 Ohm to V_{GPIO_SPI}	2			MHz
I_{out}	Output current	V_{out}=1.65V			10	mA
I_{short_max}	Short circuit current		12	20		mA
Slew	Slew rate	I_{load}= 0 C_{LOAD}=100pF	1.3	1.75		V/µs

1. V_{ICM} is the input common mode voltage.

17.3 Operational amplifiers used as comparators specifications

To use the operational amplifiers as comparators the user must disable internal compensation writing a logic one in the OpXDisComp bit in the OpAmpXCtrl register.

Table 61. Configurable 3.3V operational amplifier used as comparator specification
(Note: V_{GPIO_SPI}=3.3V unless otherwise specified)

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{GPIO_SPI}	Supply voltage range		3.15		3.45	V
V_{ICM}	Input Common Mode Voltage Range		0		V_{GPIO_SPI}	V
V_{OUT_MAX}	Output voltage	I_{load} =± 10mA	0.3		2.9	V
$I_{in\ \_offs}$	Input offset current				150	nA
$I_{in\ \_bias}$	Input bias current				500	nA
$V_{in\ \_offs}$	Input offset voltage		-5		5	mV
I_{short_max}	Short circuit current		12	20		mA
t_{PHL}	Output falling delay	V_{CM} = 1.65V Δ Vi = -/+ 20mV C_{LOAD}=100pF(1)(2)			1	µs
t_{FALL}	Fall time	V_{CM} = 1.65V Δ Vi = -/+ 20mV C_{LOAD}=100pF(1)(2)			0.4	µs
t_{PLH}	Output rising delay	V_{CM} = 1.65V Δ Vi = -/+ 20mV C_{LOAD}=100pF(1)(2)			0.5	µs
t_{RISE}	Rise time	V_{CM} = 1.65V Δ Vi = -/+ 20mV C_{LOAD}=100pF(1)(2)			0.4	µs

1. ΔVi is the differential voltage applied to input pins across the common voltage V_{CM}.
2. Measured between 50% of input and output signal.

18 Low voltage power switches

18.1 Overview

Low voltage power switches are analog switches designed to operate from a single +2.4V to +3.6V V_{GPIO_SPI} supply. They are intended to provide and remove power supply to low voltage devices. When switched on, they connect the V_{GPIO_SPI} pin to their output pin (GPIO[6] for low voltage power switch 1 or GPIO[7] for low voltage power switch 2) thus powering the device connected to it. The turning on and off of each switch can be controlled through serial interface.

S.A.B.Re provides a total of 2 low voltage power switches, each of them has current limitation to minimum 150mA to limit inrush current when charging a capacitive load. When the limit current has been reached, for more than a Tfilter time, then a flag is activated; this flag is latched in the central logic and can be cleared by the firmware. Please note that, in case of capacitive load, the current limit is reached the first time the low power switch is turned on: therefore the user will find a limit flag that must be cleared.

The 2 low voltage power switches can be externally paralleled to obtain a single super low voltage power switch. Low voltage pass switches sink current IPASS needed for their functionality from pin V_{GPIO_SPI}, they never inject current on this pin.

Figure 25. Low power switch block diagram

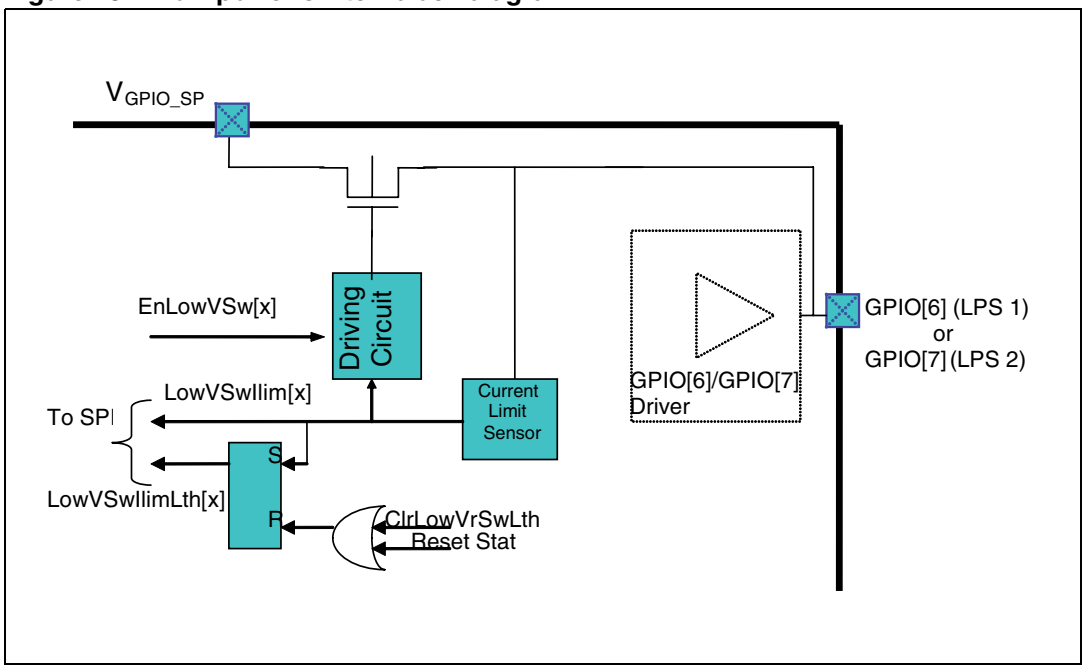


Table 62. 3.3V low power switch specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{PSW}	Input voltage range		2.4		3.6	V
V_{OUT_MAX}	Output voltage				V_{GPIO_SPI}	V
R_{DSON}	On resistance	I_{load}=100mA			1	O
I_{LIMIT}	Current limit		150	250	350	mA
$t_{deglitch}$	Current limit deglitch time		50			ns
t_{I_lim}	Current limit response time				650	ns
C_{LOAD}	Max load capacitance				2.5	µF
t_{ON}	On delay	V_{GPIO_SPI}=3.3V I_{LOAD}=1mA C_{LOAD}=100pF(1)			650	ns
t_{OFF}	Off delay	V_{GPIO_SP}I=3.3V I_{LOAD}=1mA C_{LOAD}=100pF(1)			450	ns

1. Time measured from change in SPI interface to 50% of external pin transition.

19 General purpose PWM

19.1 Overview

S.A.B.Re includes three general purpose PWM generators that can be redirected on GPIO pins (see *Chapter 23*). Two of these generators (Aux_PWM_1 and Aux_PWM_2) work with a fixed period FOSC/512 and have a programmable duty cycle; the other one (GP_PWM) has a programmable base time clock and a programmable time for both high and low levels.

19.2 General purpose PWM generators 1 and 2 (AuxPwm1 and AuxPwm2)

The Duty cycle of these PWM generators can be changed by writing the AuxPwmXCtrl bits (where X can be 1 or 2) in the AuxPwm1Ctrl and AuxPwm2Ctrl registers. Their positive duty cycle will change according to the equation:

$$PWM\_X\_DUTY = AuxPwmXCtrl[9:0]/512$$

According to this equation a programmed “0” value will cause a 0% duty cycle (output always at logic level 0).

19.3 Programmable PWM generator (GpPwm)

GpPWM has a programmable base clock that can be changed by programming the GpPwmBase[6:0] bits in the GpPwmBase register. The clock will change according to the equation:

$$PWM\_BASE\_PERIOD = (GpPwmBase[6:0] + 1) \times Tosc$$

The high and low level duration (expressed in base clock periods), can be programmed writing the GpPwmHigh[7:0] and GpPwmLow[7:0] bits in the GpPwmCtrl register so they will change according to following equations:

$$High\_level\_Time = GpPwmHigh[7:0] \times PWM\_BASE\_PERIOD$$

$$Low\_level\_Time = GpPwmLow[7:0] \times PWM\_BASE\_PERIOD$$

The resulting period of the PWM will be:

$$Period = (GpPwmHigh[7:0] + GpPwmLow[7:0]) + PWM\_BASE\_PERIOD$$

and the positive duty cycle will result:

$$DutyCycle = \frac{High\_level\_Time}{High\_level\_Time + Low\_level\_Time} = \frac{GpPwmHigh[7:0]}{GpPwmHigh[7:0] + GpPwmLow[7:0]}$$

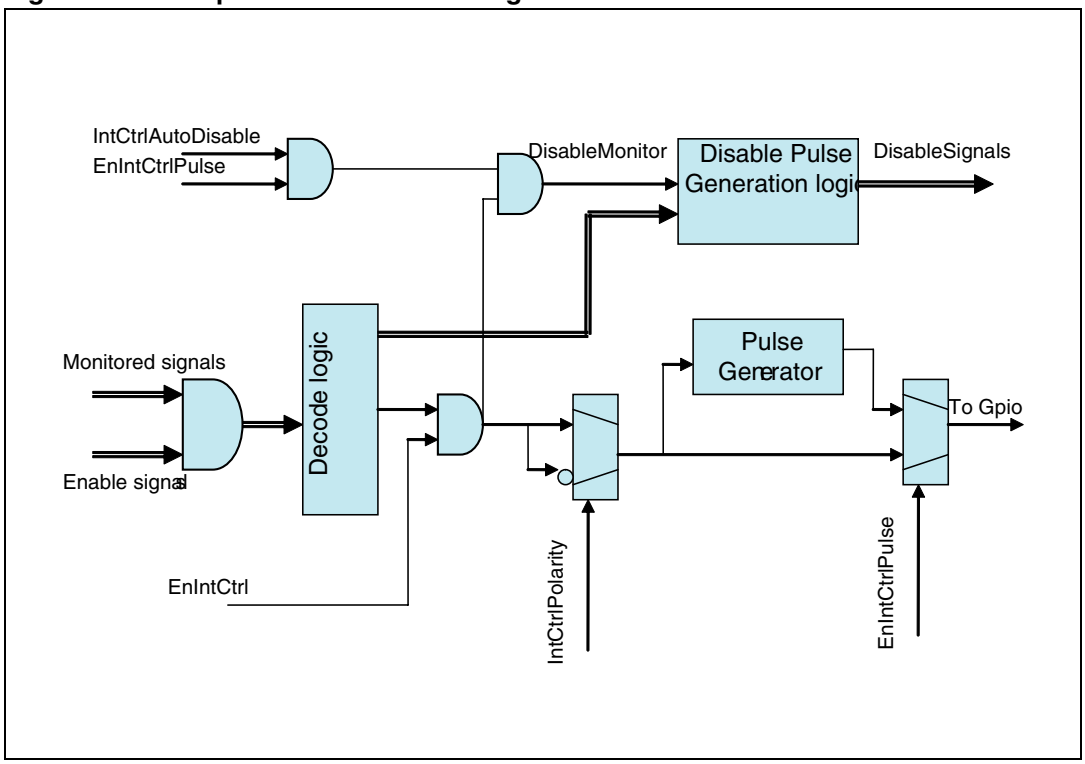
A programmed value of 0 in GpPwmHigh[7:0] and GpPwmLow[7:0] bits will force the PWM generator output to be always at logic level “0”.

20 Interrupt controller

20.1 Overview

S.A.B.Re contains one programmable interrupt controller that can be used to advice the firmware, through the serial interface, when a certain event happens inside the IC. The output of the interrupt circuit can be also redirected on a GPIO pin therefore the event can be signaled directly to the external circuits.

Figure 26. Low power switch block diagram



20.2 Interrupt controller monitored signal

The table here below contains the events that can be monitored by the interrupt controller.

Table 63. Interrupt controller event

Event	Event description	Notes
Mtr1Fault	Bridge 1 fault (Ilimit event)	
Mtr2Fault	Bridge 2 fault (Ilimit event)	
Mtr3Fault	Bridge 3 fault (Ilimit event)	
Mtr4Fault	Bridge 4 fault (Ilimit event)	
nAWAKE	nAWAKE pin low	
SwRegCtrl Ilimit	Switching regulator controller Ilimit event.	
VMainSW Ilimit	Main switching regulator Ilimit event.	
LowPowSw 1	Low voltage power switch 1 Ilimit event.	
LowPowSw 2	Low voltage power switch 2 Ilimit event	
Warm	Warming event	
WDWarn	Watch dog warning event	
WD	Watch dog event	
DigCmp	Digital comparator	
ADCDone1	ADC conversion done 1	(1)
ADCDone2	ADC conversion done 2	(1)
Vloop1Ilim	AUX1 Ilimit event.	

1. This event is disabled if the related ADC channel is configured in continuous mode.

Any event detection can be enabled and disabled by setting at logic level 1 the relative enable bit in the interrupt controller configuration register (IntCrtlCfg).

The interrupt controller can be programmed to give a pulse when a monitored event happens or to continuously maintaining the output active until the interrupt condition is finished.

When programmed to signal the enabled events by giving pulses, the interrupt controller can be configured to disable the event that caused the interrupt request until the firmware re-enables it writing the relative bit in the control register (IntCrtlCtrl) or to continue to monitor the event.

The GPIO output of this circuit can be programmed to be active high or active low.

Table 64. Interrupt controller specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
t_{PULSE}	Pulse duration			16*Tosc		µs
$t_{INTFILT}$	Filter time			200		ns

21 Digital comparator

21.1 Overview

S.A.B.Re includes one digital comparator that can be used to signal, through serial interface, that a channel converted by the ADC is greater, greater-equal, lesser, lesser equal, or equal than a fixed value set by serial interface or than the value converted by the other ADC channel.

This circuit can be used to monitor the temperature of the IC advising the firmware when it reaches a certain value decided by the firmware by setting one ADC channel to do continuous conversions of the temperature sensor.

The circuit operation can be enabled or disabled changing the EnDigCmp bit in the configuration register DigCmpCfg. By setting the DigCmpUpdate[1:0] bits in the configuration register, the comparator can be programmed to update its output in one of the following ways:

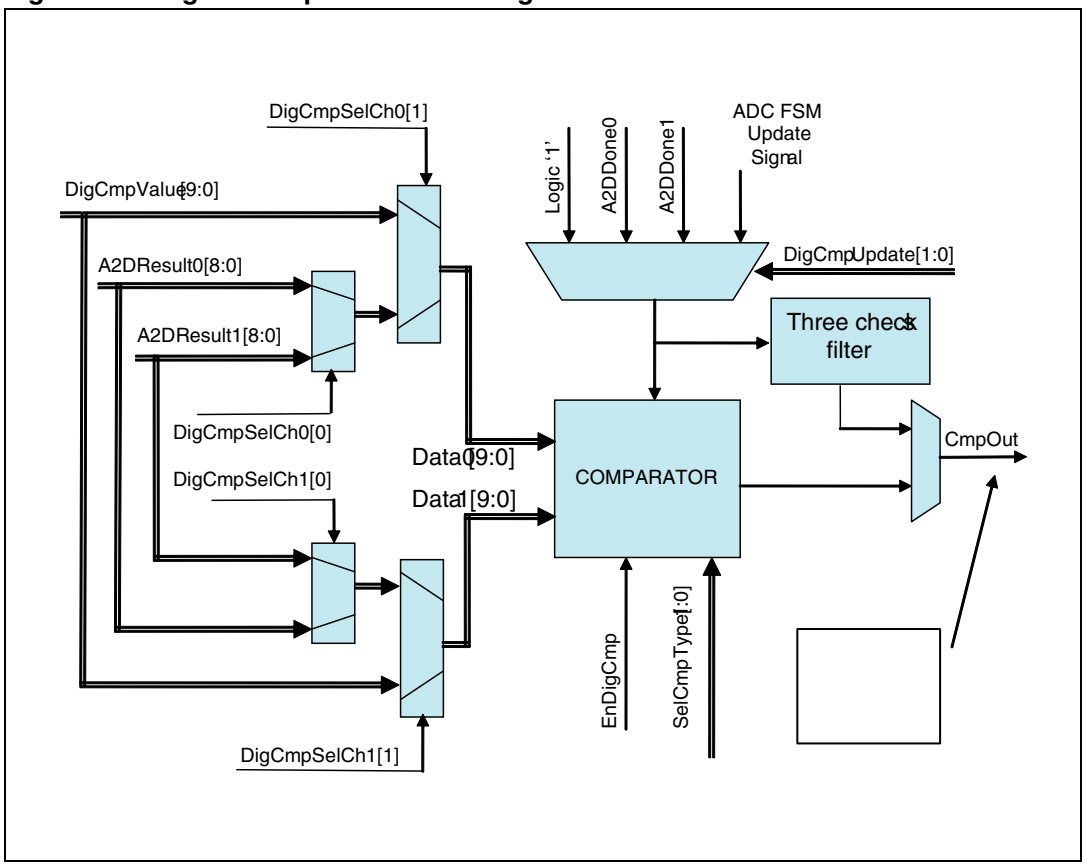
- DigCmpUpdate[1:0]=00
  - Continuously (each clock).
- DigCmpUpdate[1:0]=01
  - Each time a conversion is performed on ADC channel 0.
- DigCmpUpdate[1:0]=10
  - Each time a conversion is performed on ADC channel 1.
- DigCmpUpdate[1:0]=11
  - ADC state machine driven.

When the last option is selected, the digital comparator will update its output in two different ways depending on the configuration of the ADC converter. If ADC converter is configured to do continuous conversions on both channels, the output of the comparator will be updated when the double conversion is completed. If ADC converter is not configured to do continuous conversions on both channels, the output of the comparator will be updated each time a conversion is completed.

The comparator output can be digitally filtered so that the programmed condition has to be found for three consecutive checks before to be signaled.

The picture here below is a block representation of the comparator.

Figure 27. Digital Comparator block diagram



Here below is reported the comparison type truth table:

Table 65. Comparison type truth

EnDigCmp	SelCmpType[1]	SelCmpType[0]	Comparison type
0	X	X	Disabled
1	0	0	Data0[9:0] ≤1³1÷Data1[9:0]
1	0	1	Data0[9:0] = Data1[9:0]
1	1	0	Data0[9:0] > Data1[9:0]
1	1	1	Data0[9:0] ≤= Data1[9:0]

Here below is reported the Data0/Data1 selection truth table:

Table 66. DataX selection truth

DigCmpSelChX[1]	DigCmpSelChX[0]	DataX[9:0]
0	X	DigCmpValue[9:0]
1	0	A2DResult1[8:0]
1	1	A2DResult1[8:0]

22 GPIO pins

22.1 Overview

Some of the pins of S.A.B.Re are indicated as GPIO (General Purpose I/O). These pins can be configured to be used in different ways depending on customer application. All GPIOs can be used as digital input/output pins with digital value settable/readable using serial interface or as analog input pins that can be converted using the A2D system. Some of the pins can be used for special purposes: i.e. two of them can be used to access to the pass switch function, other two are used as feedback pins for the auxiliary synchronous switching regulators.

All input Schmitt triggers and output circuitry used for start-up purposes are powered by the internally generated V_{3v3}, while the digital output buffers are powered by V_{GPIO_SPI} pin. To ensure independency between V_{3v3} and V_{GPIO_SPI} the GPIOs output drivers are open-drain driver or the high side MOS is in back-to-back configuration to avoid the presence of the body diode between output and supply (all back-to-back drivers can be customized to become open-drain drivers with a metal change).

All digital output signals can be inverted before being provided on the relative GPIO pins.

Here below is reported the table with GPIO functions:

Table 67. GPIO functions description

Pin Name	Function(1)					Notes
	Input		Output		Special	
	Analog	Digital	Analog	Digital		
GPIO[0]	- ADC input	- SPI IN		- SPI OUT - Interrupt ctrl. - AuxPwm1 - AuxPwm2	Start-up configuration pin	Open drain output
GPIO[1]	- ADC input - Comp1 In- - Vaux1 F.B.	- SPI IN		- SPI OUT - Interrupt ctrl. - AuxPwm1 - AuxPwm2		Open drain output
GPIO[2]	- ADC input - Comp2 In- - Vaux2 F.B.	- SPI IN - IN PWM		- SPI OUT - Interrupt ctrl. - AuxPwm2 - AuxPwm3		Open drain output
GPIO[3]	- ADC input	- SPI IN		- SPI OUT - AuxPwm2 - AuxGpPwm3	Start-up configuration pin	Open drain output
GPIO[4]	- ADC input	- SPI IN		- SPI OUT - Interrupt ctrl. - AuxPwm1 - AuxPwm3	Start-up configuration pin	Open drain output

Table 67. GPIO functions description (continued)

Pin Name	Function[1]					Notes
	Input		Output		Special	
	Analog	Digital	Analog	Digital		
GPIO[5]	- ADC input	- SPI IN		- SPI OUT - Reg. loop 1 - Comp1 out - AuxPwm3	Slave Control	Full driver BB powered by V_{3v3}
GPIO[6]	- ADC input	- SPI IN	- Low Pow Sw 1	- SPI OUT - A2DGpo - AuxPwm2 - Comp2 out		Full driver connected to V_{GPIO_SPI}
GPIO[7]	- ADC input	- SPI IN	- Low Pow Sw 2	- SPI OUT - AuxPwm1 - AuxPwm3 - Comp1 out		Full driver connected to V_{GPIO_SPI}
GPIO[8]	- ADC input	- SPI IN[2]	- CurrDAC	- SPI OUT - AuxPwm1 - AuxPwm3 - Comp2 out	5 volt input tolerant	Open drain output
GPIO[9]	- ADC input - OpAmp1 in+	- SPI IN - ID 1 - IN PWM		- SPI OUT - Interrupt contr. - AuxPwm1 - Reg. loop 3		Full driver connected to V_{GPIO_SPI}
GPIO[10]	- ADC input - OpAmp1 in-	- SPI IN - ID 2 - IN PWM		- SPI OUT - Interrupt ctrl. - AuxPwm2 - AuxPwm3		Full driver connected to V_{GPIO_SPI}
GPIO[11]	- ADC input	- SPI IN - IN PWM	- OpAmp1 Out	- SPI OUT - A2DGpo - AuxPwm1 - AuxPwm2		Full driver connected to V_{GPIO_SPI}
GPIO[12]	- ADC input - OpAmp2 in+	- SPI IN - STEP_REQ		- SPI OUT - Interrupt ctrl - Comp2 out - Reg. loop 2		Full driver BB (can be powered by V_{3v3} with a metal change)

Table 67. GPIO functions description (continued)

Pin Name	Function(1)					Notes
	Input		Output		Special	
	Analog	Digital	Analog	Digital		
GPIO[13]	- ADC input - OpAmp2 in-	- SPI IN		- SPI OUT - AuxPwm1 - Reg. loop 3 - AuxPwm3		Full driver connected to V_{GPIO_SPI}
GPIO[14]	- ADC input	- SPI IN	- OpAmp2 Out	- SPI OUT - Interrupt ctrl. - AuxPwm2 - AuxPwm3		Full driver connected to V_{GPIO_SPI}

1. In the above table the following abbreviations were used.
2. Gpio[8] input Schmitt trigger is disabled by default (after a reset) to be able to read the digital value from this pin it needs to be enabled writing a logic '1' in the EnGpio8DigIn in CurrDacCtrl register.

Table 68. Abbreviations

Abbreviation	Meaning
ADC input	Input to the ADC system.
SPI IN	Digital state of this pin is readable through SPI.
SPI OUT	Digital state of this pin can be set through SPI.
BB	Back to back high side driver.
Comp1 IN -	This pin can be used as minus input for comparator 1.
Comp2 IN -	This pin can be used as minus input for comparator 2.
Vaux1 FB	This pin can be used as feedback input for AUX1 regulator obtained by using bridge 3.
A2DGpo	This pin can be used to carry out the A2DGpo value related to the ADC conversion S.A.B.Re is doing.
Reg. Loop 3	This pin can be used as output of the regulation loop used by AUX3 regulator obtained by using bridge 4.
STEP_REQ	This pin can be used to request a stepper sequencer evolution step.
Interrupt Ctrl	This pin can be used to carry out the interrupt controller circuit output.
Vaux2 FB	This pin can be used as feedback pin by AUX2 regulator obtained by using bridge 3
IN PWM	This pin can be used to provide an external PWM to bridges.
Reg. Loop 1	This pin can be used as output of the regulation loop used by AUX1 regulator.
Comp1 OUT	This pin can be used as output of the comparator 1.
AuxPwm1	This pin can be used to carry out the PWM generated by AuxPwm1 circuit.
Low Volt. Pow. Sw. 1	This pin can be used as output of low voltage power switch 1.

Table 68. Abbreviations (continued)

Abbreviation	Meaning
Reg. Loop 2	This pin can be used as output of the regulation loop used by AUX2 regulator.
Comp2 OUT	This pin can be used as output of the comparator 2.
AuxPwm2	This pin can be used to carry out the PWM generated by AuxPwm2 circuit.
Low Volt. Pow. Sw. 2	This pin can be used as output of low voltage power switch 2.
Reg. Loop 3	This pin can be used as output of the regulation loop used by AUX3 regulator.
AuxPwm3	This pin can be used to carry out the PWM generated by AuxPwm3 circuit.
CurrDAC	This pin can be used to carry out the output of the current DAC circuit.
AuxPwm4	This pin can be used to carry out the PWM generated by AuxPwm4 circuit.
OpAmp1 in+	This pin can be used as operational amplifier 1 non-inverting input.
OpAmp1 in-	This pin can be used as operational amplifier 1 inverting input.
OpAmp1 Out	This pin can be used as operational amplifier 1 output.
OpAmp2 in+	This pin can be used as operational amplifier 2 non-inverting input.
OpAmp2 in-	This pin can be used as operational amplifier 2 inverting input.
OpAmp2 Out	This pin can be used as operational amplifier 2 output.
ID 1	This pin is used to determine the SPI ID1 bit value.
ID 2	This pin is used to determine the SPI ID2 bit value.
Slave Control	This pin is used as slave control when the IC is configured as master.

Hereafter are reported the detailed specifications for each GPIO.

To enable the functionality of the GPIO as output pin, the relative GpioOutEnable[14:0] bit must be enabled in GpioOutEnable register.

Each GPIO could be configured by setting the appropriate GpioXMode[2:0] in the GpioCtrlX register.

22.2 GPIO[0]

The GPIO[0] truth table is (for the abbreviation list please refer to *Table 68*):

Table 69. GPIO[0] truth

State at StartUp	GPIO[0] SPI BITS				Function	Note
	GpioOut Enable [0]	Mode[2]	Mode[1]	Mode[0]		
1	X	X	X	X	Detection of StartUp config	See *Chapter 8*
0	0	X	X	X	HiZ (SPI_IN)	
0	1	0	0	0	SPI OUT	(1)
0	1	0	0	1	InterruptCtrl	(1)
0	1	0	1	0	AuxPwm1	(1)
0	1	0	1	1	AuxPwm2	(1)
0	1	1	0	0	SPI OUT inverted	(1)
0	1	1	0	1	InterruptCtrl inverted	(1)
0	1	1	1	0	AuxPwm1 inverted	(1)
0	1	1	1	1	AuxPwm2 inverted	(1)

1. In all configurations in which GPIO[0] is enabled as output:
   a) the GPIO[0] pin can be always used as an analog input to the ADC system (ADC function) by writing its address in the A2DChannelX[4:0] in the A2DConfigX register and starting a conversion;
   b) the GPIO[0] pin can be always used as a digital input so its value can be always read through SPI interface (SPI_IN function);
   c) the GPIO[0] pin is an open drain output.

Figure 28. GPIO[0] block diagram

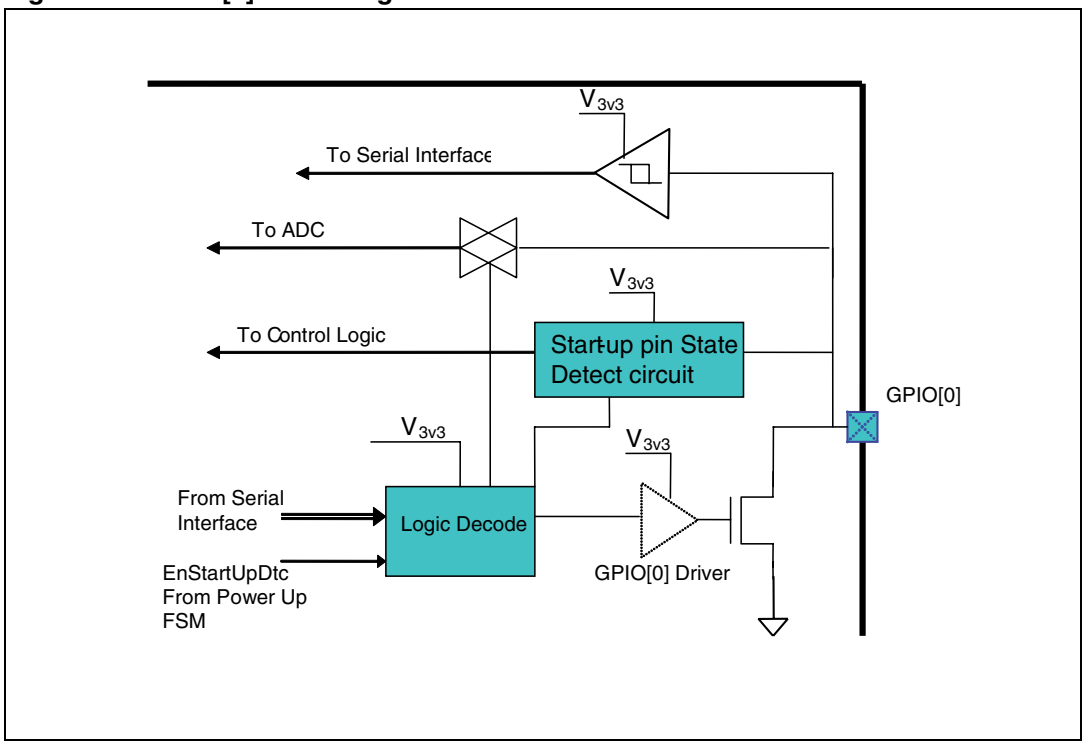


Table 70. GPIO[0] specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Input voltage hysteresis			0.22		V
V_{OL}	Low level output voltage	I_{OUT} = 15mA			0.4	V
$I_{LEAKAGE}$	Leakage current	0 ≤Vout ≤ V_{3v3}	-1		1	µA
C_{LOAD}	Load capacitance				200	pF
t_{DELAY}	Delay from serial write to pin Low	C_{LOAD} =50 pF(1)			500	ns

1. Measured between nSS rising edge and 50% of V_{out}.

22.3 GPIO[1]

The GPIO[1] truth table is (for the abbreviation list please refer to *Table 68*):

Table 71. GPIO[1] truth

AUX1Enable or AUX1System	GPIO[1] SPI BITS				Function	Note
	GpioOut Enable [1]	Mode[2]	Mode[1]	Mode[0]		
1	X	X	X	X	AUX1 FB	(1)
0	0	0	X	X	HiZ (SPI_IN)	
0	0	1	X	X	Comp1 IN -	(2)
0	1	0	0	0	SPI OUT	(2)
0	1	0	0	1	AuxPwm1	(2)
0	1	0	1	0	AuxPwm2	(2)
0	1	0	1	1	InterruptCtrl	(2)
0	1	1	0	0	SPI OUT inverted	(2)
0	1	1	0	1	AuxPwm1 inverted	(2)
0	1	1	1	0	AuxPwm2inverted	(2)
0	1	1	1	1	IntCtrlinverted	(2)

1. AUX1Enable or AUX1System bit =1 represent the case in which AUX1 is used as a System or Not System regulator.
2. In all configurations in which GPIO[1] is enabled as output:
   a) the GPIO[1] pin can be always used as an analog input to the ADC system (ADC function) by writing its address in the A2DChannelX[4:0] in the A2DConfigX register and starting a conversion;
   b) the GPIO[1] pin can be always used as a digital input so its value can be always read through SPI interface (SPI_IN function);
   c) the GPIO[1] pin is an open drain output.

Figure 29. GPIO[1] block diagram

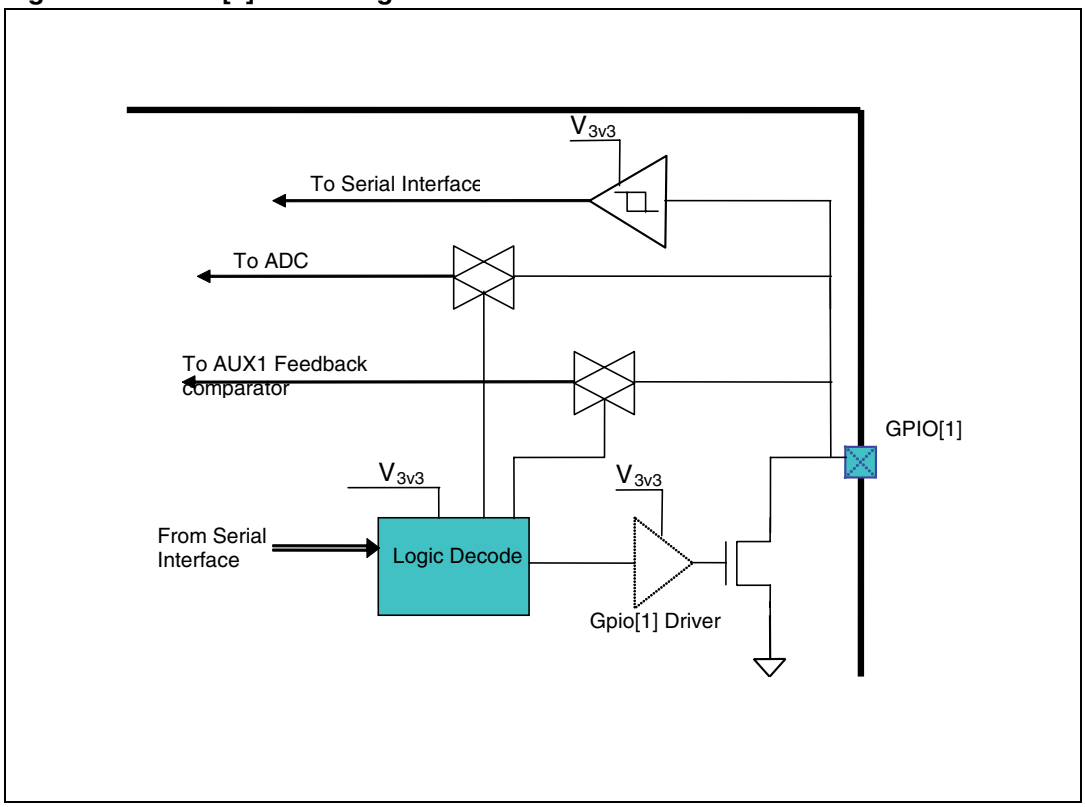


Table 72. GPIO[1] specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Input voltage hysteresis			0.22		V
V_{OL}	Low level output voltage	I_{OUT} = 15mA			0.4	V
$I_{LEAKAGE}$	Leakage current	$0 \leq V_{out} \leq V_{3v3}$	-1		1	µA
t_{DELAY}	Delay from serial write to pin low	C_{LOAD} =50 pF(1)			500	ns

1. Measured between nSS rising edge and 50% of V_{out}.

22.4 GPIO[2]

The GPIO[2] truth table is (for the abbreviation list please refer to *Table 68*):

Table 73. GPIO[2] truth

AUX2Enable or AUX2System	GPIO[1] SPI BITS				Function	Note
	GpioOut Enable [1]	Mode[2]	Mode[1]	Mode[0]		
1	X	X	X	X	AUX2 FB	(1)
0	0	0	X	X	HiZ (SPI_IN)	
0	0	1	X	X	Comp1 IN -	(2)
0	1	0	0	0	SPI OUT	(2)
0	1	0	0	1	AuxPwm2	(2)
0	1	0	1	0	AuxPwm3	(2)
0	1	0	1	1	InterruptCtrl	(2)
0	1	1	0	0	SPI OUT inverted	(2)
0	1	1	0	1	AuxPwm2 inverted	(2)
0	1	1	1	0	AuxPwm3 inverted	(2)
0	1	1	1	1	IntCtrlinverted	(2)

1. AUX2Enable or AUX2System bit =1 represent the case in which AUX1 is used as a System or Not System regulator.
2. In all configurations in which GPIO[2] is enabled as output:
   a) the GPIO[2] pin can be always used as an analog input to the ADC system (ADC function) by writing its address in the A2DChannelX[4:0] in the A2DConfigX register and starting a conversion;
   b) the GPIO[2] pin can be always used as a digital input so its value can be always read through SPI interface (SPI_IN function);
   c) please note that GPIO[2] output is directly connected to ExtPWM3 input for Bridge 3 or 4 and therefore particular care must be taken in order to avoid wrong PWM signals when ExtPWM3 is selected for bridge 3 or 4;
   d) the GPIO[2] pin is an open drain output.

Figure 30. GPIO[2] block diagram

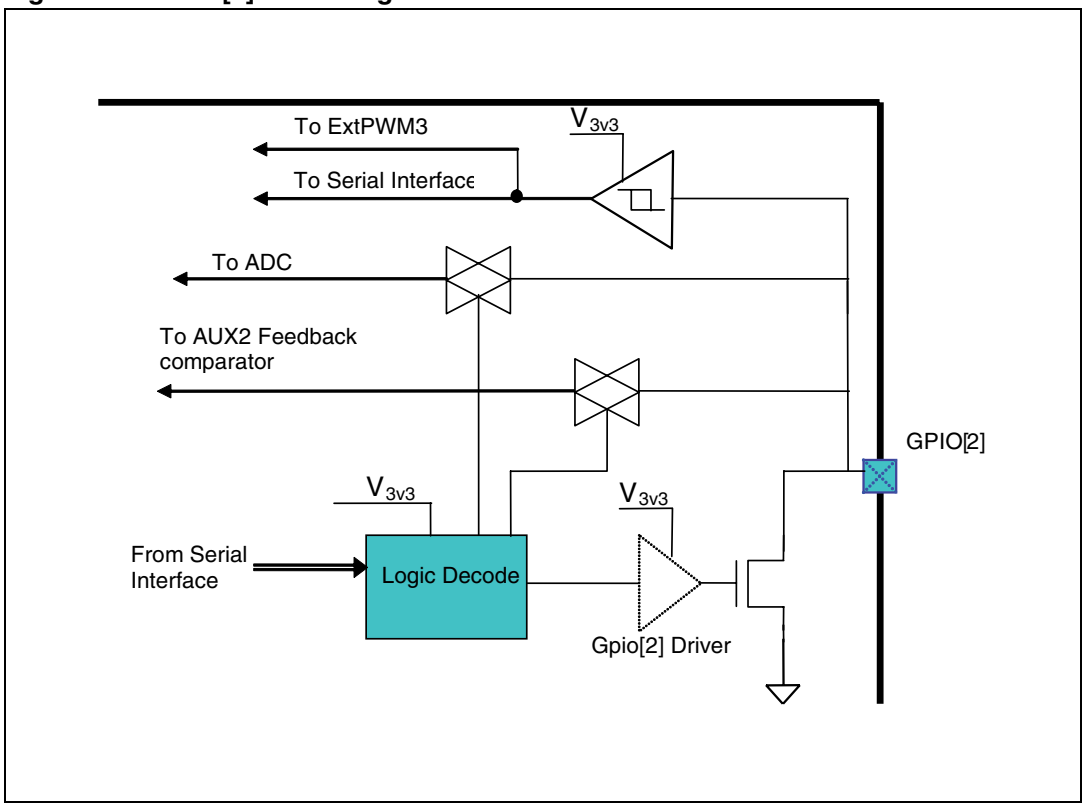


Table 74. GPIO[2] specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Input voltage hysteresis			0.22		V
V_{OL}	Low level output voltage	I_{OUT} = 15mA			0.4	V
$I_{LEAKAGE}$	Leakage current	$0 \le V_{out} \le V_{3v3}$	-1		1	µA
t_{DELAY}	Delay from serial write to pin low	C_{LOAD} =50 pF(1)			500	ns

1. Measured between nSS rising edge and 50% of V_{out}.

22.5 GPIO[3]

The GPIO[3] truth table is (for the abbreviation list please refer to *Table 68*):

Table 75. GPIO[3] truth

State at StartUp	GPIO[3] SPI BITS				Function	Note
	GpioOut Enable [3]	Mode[2]	Mode[1]	Mode[0]		
1	X	X	X	X	Detection of StartUp config	See *Chapter 8*
0	0	X	X	X	HiZ (SPI_IN)	
0	1	0	0	0	SPI OUT	(1)
0	1	0	0	1	AuxPwm1	(1)
0	1	0	1	0	AuxPwm2	(1)
0	1	0	1	1	AuxPwm2	(1)
0	1	1	0	0	SPI OUT inverted	(1)
0	1	1	0	1	AuxPwm1 inverted	(1)
0	1	1	1	0	AuxPwm2 inverted	(1)
0	1	1	1	1	AuxPwm3 inverted	(1)

1. In all configurations in which GPIO[3] is enabled as output:
   a) the GPIO[3] pin can be always used as an analog input to the ADC system (ADC function) by writing its address in the A2DChannelX[4:0] in the A2DConfigX register and starting a conversion;
   b) the GPIO[3] pin can be always used as a digital input so its value can be always read through SPI interface (SPI_IN function);
   c) the GPIO[3] pin is an open drain output.

Figure 31. GPIO[3] block diagram

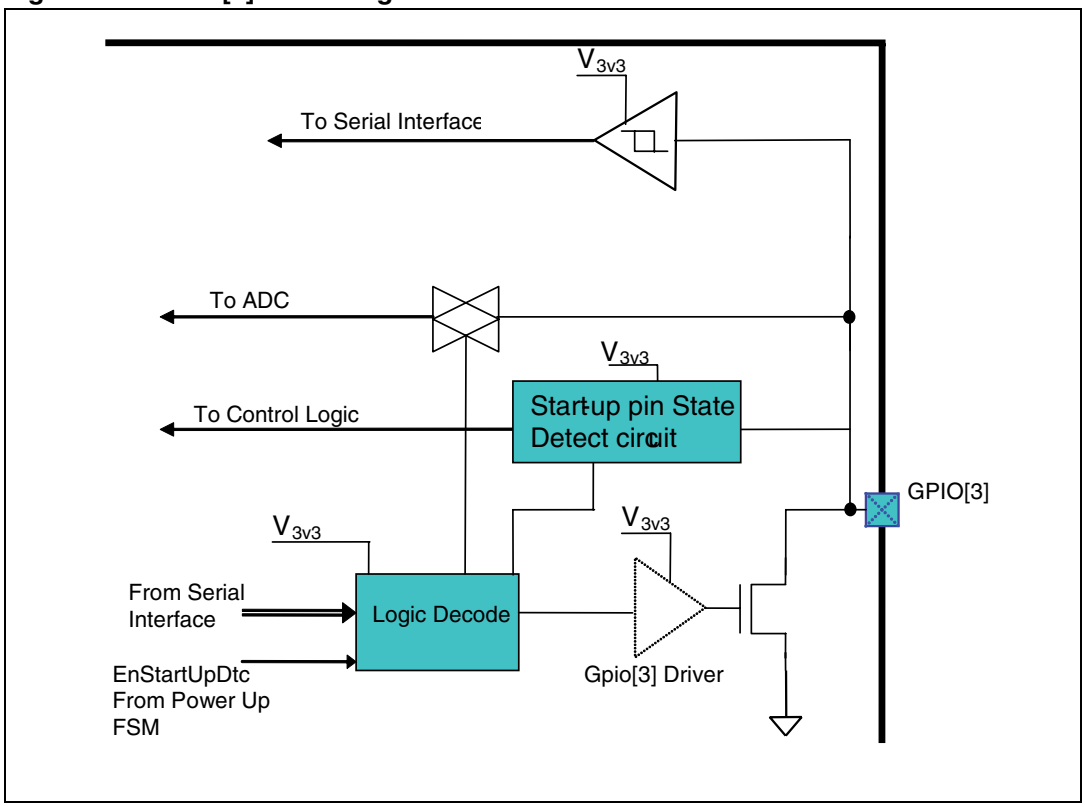


Table 76. GPIO[3] specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Input voltage hysteresis			0.22		V
V_{OL}	Low level output voltage	I_{OUT} = 15mA			0.4	V
$I_{LEAKAGE}$	Leakage current	$0 \leq V_{out} \leq V_{3v3}$	-1		1	µA
C_{LOAD}	Load capacitance				200	pF
t_{DELAY}	Delay from serial write to pin low	C_{LOAD} =50 pF(1)			500	ns

1. Measured between nSS rising edge and 50% of V_{out}.

22.6 GPIO[4]

The GPIO[4] truth table is (for the abbreviation list please refer to *Table 68*):

Table 77. GPIO[4] truth

State at StartUp	GPIO[4] SPI BITS				Function	Note
	GpioOut Enable [4]	Mode[2]	Mode[1]	Mode[0]		
1	X	X	X	X	Detection of StartUp config	See *Chapter 8*
0	0	X	X	X	HiZ (SPI_IN)	
0	1	0	0	0	SPI OUT	(1)
0	1	0	0	1	Interrupt Ctrl	(1)
0	1	0	1	0	AuxPwm1	(1)
0	1	0	1	1	AuxPwm3	(1)
0	1	1	0	0	SPI OUT inverted	(1)
0	1	1	0	1	Interrupt Ctrl	(1)
0	1	1	1	0	AuxPwm1 inverted	(1)
0	1	1	1	1	AuxPwm3 inverted	(1)

1. In all configurations in which GPIO[4] is enabled as output:
   a) the GPIO[4] pin can be always used as an analog input to the ADC system (ADC function) by writing its address in the A2DChannelX[4:0] in the A2DConfigX register and starting a conversion;
   b) the GPIO[4] pin can be always used as a digital input so its value can be always read through SPI interface (SPI_IN function);
   c) the GPIO[4] pin is an open drain output.

Figure 32. GPIO[4] block diagram

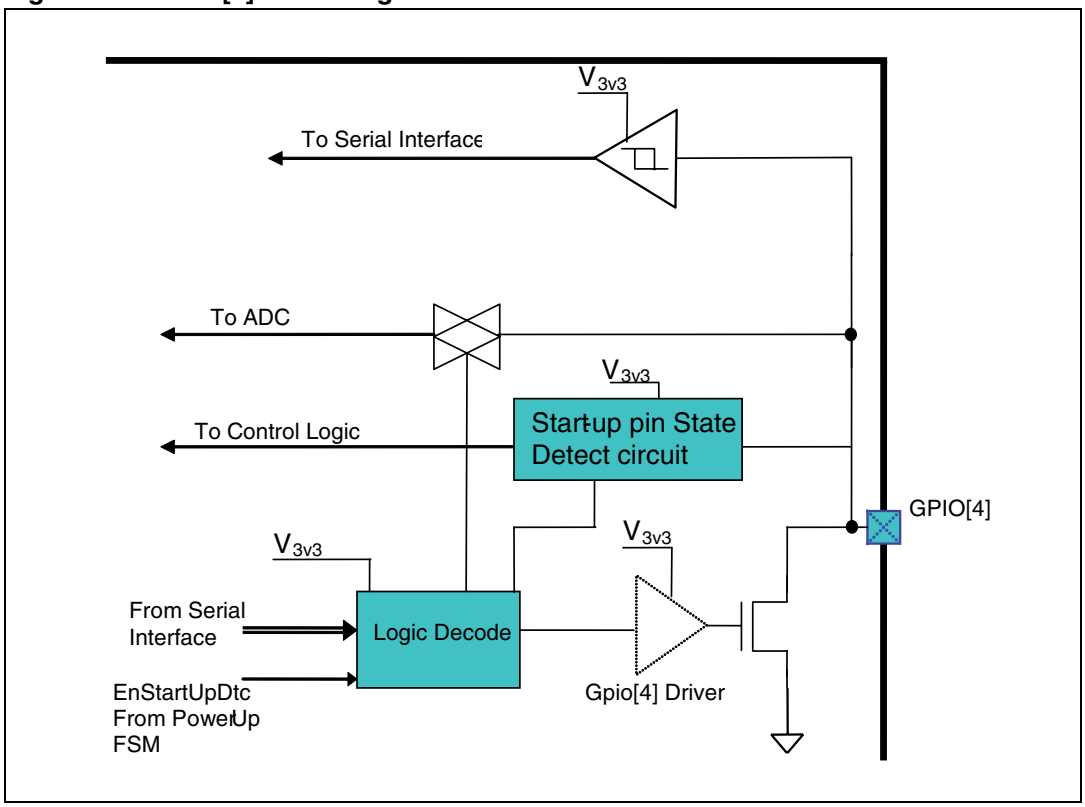


Table 78. GPIO[4] specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Input voltage hysteresis			0.22		V
V_{OL}	Low level output voltage	I_{OUT} = 15mA			0.4	V
$I_{LEAKAGE}$	Leakage current	$0 \leq V_{out} \leq V_{3v3}$	-1		1	µA
C_{LOAD}	Load capacitance				200	pF
t_{DELAY}	Delay from serial write to pin low	C_{LOAD} =50 pF(1)			500	ns

1. Measured between nSS rising edge and 50% of V_{out}.

22.7 GPIO[5]

The GPIO[5] truth table is (for the abbreviation list please refer to *Table 68*):

Figure 33. GPIO[5] block diagram

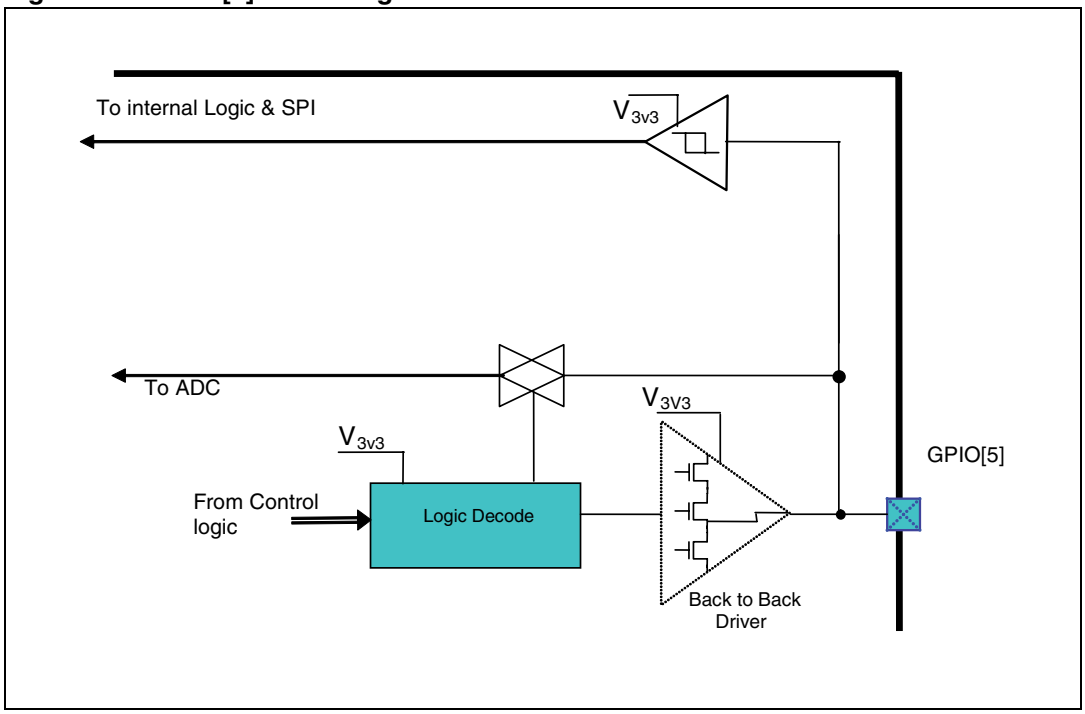


Table 79. GPIO[5] truth

Master(1)	AUX1 system and Vloop1 external(2)	GPIO[5] SPI BITS				Function	Note
		GpioOut enable[5]	Mode[2]	Mode[1]	Mode[0]		
1	X	X	X	X	X	Slave control	
0	1	X	X	X	X	Reg Loop1 OUT	(3)
0	0	0	X	X	X	HiZ (SPI_IN)	
0	0	1	0	0	0	SPI OUT	(3)
0	0	1	0	0	1	Comp1OUT	(3)
0	0	1	0	1	0	Reg Loop1 OUT	(3)
0	0	1	0	1	1	AuxPwm3	(3)
0	0	1	1	0	0	SPI OUT inverted	(3)
0	0	1	1	0	1	Comp1OUT inverted	(3)
0	0	1	1	1	0	Reg Loop1 OUT inverted	(3)
0	0	1	1	1	1	AuxPwm3 inverted	(3)

1. Master bit is at logic level “1” when S.A.B.Re is used as a master device (see *Chapter 8*)

2. This bit is at logic level “1” if AUX1 regulator is a system regulator but its power stage is externally realized (and therefore the regulation loop is not used to drive bridge 3). In this case Vloop1IsSys bit will be at logic level “1”, while Vloop1OnMtr3SideA and Vloop1OnMtr3SideB bits will be at logic level “0” in CoreConfigReg register.
3. In all configurations in which GPIO[5] is enabled as output:
   a) the GPIO[5] pin can be always used as an analog input to the ADC system (ADC function) by writing its address in the A2DChannelX[4:0] in the A2DConfigX register and starting a conversion;
   b) the GPIO[5] pin can be always used as a digital input so its value can be always read through SPI interface (SPI_IN function);
   c) the GPIO[5] pin is a rail to rail, back to back output supplied by V_{3v3}.

Table 80. GPIO[5] specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Input voltage hysteresis			0.22		V
V_{OL}	Low level output voltage	I_{OUT} = 15mA			0.4	V
V_{OH}	High level output voltage	I_{OUT} = 5mA	2.75			V
$I_{LEAKAGE}$	Leakage current	$0 \leq V_{out} \leq V_{3v3}$	-1		1	µA
t_{DELAY}	Delay from serial write to pin low	C_{LOAD} =50 pF(1)			500	ns

1. Measured between nSS rising edge and 50% of V_{out}.

22.8 GPIO[6]

The GPIO[6] truth table is (for the abbreviation list please refer to *Table 68*):

Table 81. GPIO[6] truth

StdByMode	AEnLow VSw[1]	GPIO[6] SPI BITS				Function	Note
		GpioOut enable[6]	Mode[2]	Mode[1]	Mode[0]		
1	X	X	X	X	X	Low Volt. Pow. Sw. 1	
0	1	X	X	X	X	Low Volt. Pow. Sw. 1	(1)
0	0	0	X	X	X	HiZ (SPI_IN)	
0	0	1	0	0	0	SPI OUT	(2)
0	0	1	0	0	1	A2DGpo	(2)
0	0	1	0	1	0	AuxPwm2	(2)
0	0	1	0	1	1	Comp2OUT	(2)
0	0	1	1	0	0	A2DGpo inverted	(2)
0	0	1	1	0	1	AuxGpPwm2 inverted	(2)
0	0	1	1	1	1	Comp2OUT inverted	(2)

1. When EnLowVSw[1]= ‘1’ the GpioOutEnable[6] bit is forced to 0.
2. In all configurations in which GPIO[6] is enabled as output:
   a) the GPIO[6] pin can be always used as an analog input to the ADC system (ADC function) by writing its address in the A2DChannelX[4:0] in the A2DConfigX register and starting a conversion;
   b) the GPIO[6] pin can be always used as a digital input so its value can be always read through SPI interface (SPI_IN function);
   c) the GPIO[6] pin is a rail to rail output supplied by V_{GPIO_SPI}.

Figure 34. GPIO[6] block diagram

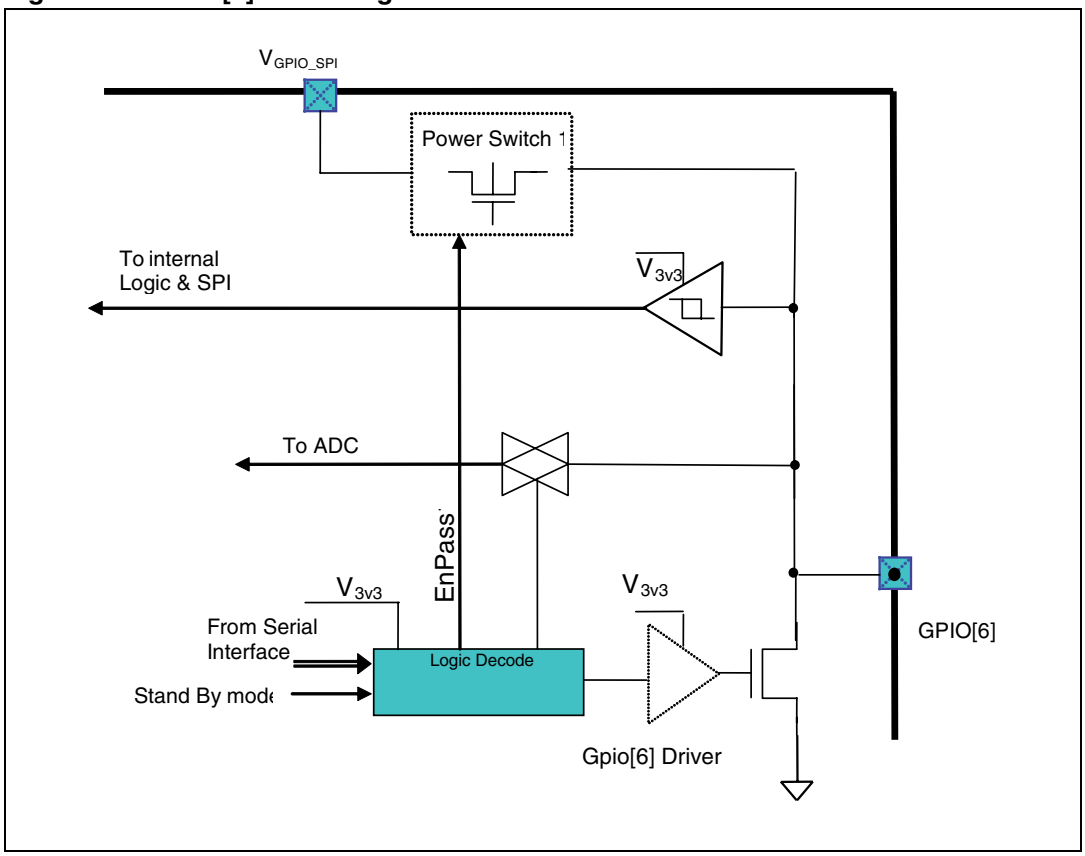


Table 82. GPIO[6] specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Input voltage hysteresis			0.22		V
V_{OL}	Low level output voltage	I_{OUT} = 15mA			0.4	V
$I_{LEAKAGE}$	Leakage current	$0 \leq V_{out} \leq V_{3v3}$	-1		1	µA
t_{DELAY}	Delay from serial write to pin low	C_{LOAD} =50 pF(1)			500	ns

1. Measured between nSS rising edge and 50% of V_{out}.

22.9 GPIO[7]

The GPIO[7] truth table is (for the abbreviation list please refer to *Table 68*):

Table 83. GPIO[7] truth

EnLowVSw[2]	GPIO[7] SPI BITS				Function	Note
	GpioOut enable[7]	Mode[2]	Mode[1]	Mode[0]		
1	X	X	X	X	Low Volt. Pow. Sw. 2	(1)
0	0	X	X	X	HiZ (SPI_IN)	
0	1	0	0	0	SPI OUT	(2)
0	1	0	0	1	AuxPwm1	(2)
0	1	0	1	0	AuxPwm3	(2)
0	1	0	1	1	Comp1OUT	(2)
0	1	1	0	0	AuxPwm1 inverted	(2)
0	1	1	0	1	AuxPwm3 inverted	(2)
0	1	1	1	1	Comp1OUT inverted	(2)

1. When EnLowVSw[2] = '1' the GpioOutEnable[7] bit is forced to 0.
2. In all configurations in which GPIO[7] is enabled as output:
   a) the GPIO[7] pin can be always used as an analog input to the ADC system (ADC function) by writing its address in the A2DChannelX[4:0] in the A2DConfigX register and starting a conversion;
   b) the GPIO[7] pin can be always used as a digital input so its value can be always read through SPI interface (SPI_IN function);
   c) the GPIO[7] pin is a rail to rail output supplied by V_{GPIO_SPI}.

Figure 35. GPIO[7] block diagram

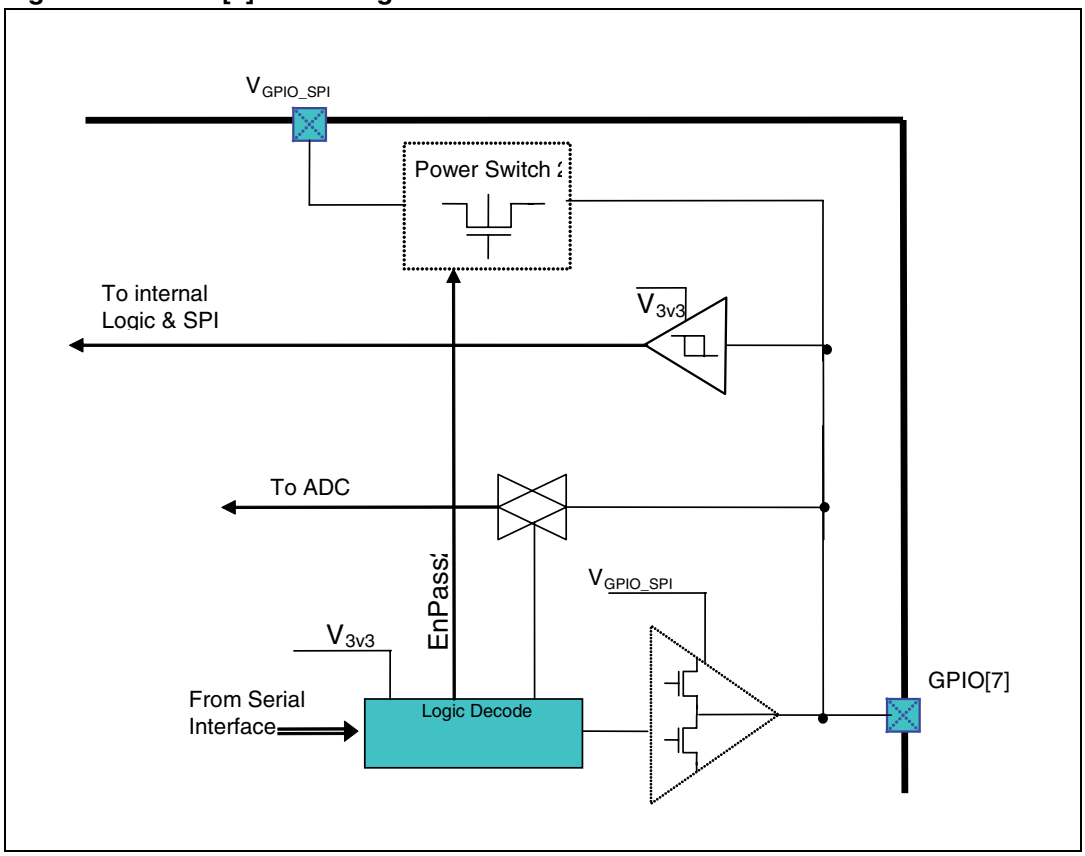


Table 84. GPIO[7] specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Input voltage hysteresis			0.22		V
V_{OL}	Low level output voltage	I_{OUT} = 15mA, V_{GPIO_SPI} = 3.15V			0.4	V
V_{OH}	High level output voltage	I_{OUT} = 15mA, V_{GPIO_SPI} = 3.15V	2.75			V
$I_{LEAKAGE}$	Leakage current	$0 \leq V_{out} \leq V_{GPIO\_SPI}$, V_{GPIO_SPI} = 3.15V	-1		1	µA
t_{DELAY}	Delay from serial write to pin low	C_{LOAD} =50 pF(1)			500	ns

1. Measured between nSS rising edge and 50% of V_{out}.

22.10 GPIO[8]

The GPIO[8] truth table is (for the abbreviation list please refer to *Table 68*):

Table 85. GPIO[8] truth

EnDac (1)	GPIO[8] SPI BITS				Function (2)	Note
	GpioOut enable[8]	Mode[2]	Mode[1]	Mode[0]		
1	X	X	X	X	CurrDAC	(3)
0	0	X	X	X	HiZ (SPI_IN)	(4)
0	1	0	0	0	SPI OUT	(4)
0	1	0	0	1	AuxPwm1	(4)
0	1	0	1	0	AuxPwm3	(4)
0	1	0	1	1	Comp2OUT	(4)
0	1	1	0	0	AuxPwm1 inverted	(4)
0	1	1	0	1	AuxPwm3 inverted	(4)
0	1	1	1	1	Comp2OUT inverted	(4)

1. The EnDAC bit in the CurrDacCtrl register enables the Current DAC (see*Chapter 17*)
2. This pin is 5 volt input tolerant.
3. When EnDAC = ‘1’ the GpioOutEnable[8] bit is forced to 0. The current DAC circuit is directly connected to GPIO[8] pin so as soon as it is enabled it will sink current from pin.
4. The GPIO[8] pin can be always used as a digital input so its value can be always read through SPI interface (SPI_IN function). To avoid affecting the precision of CurrDAC when this is used to sink very low currents, it is necessary to enable the digital input functionality of GPIO[8]. Therefore to read their values through SPI interface (SPI_IN function), it is necessary to enable the EnGpio8DigIn bit in the CurrDacCtrl register.

Figure 36. GPIO[8] block diagram

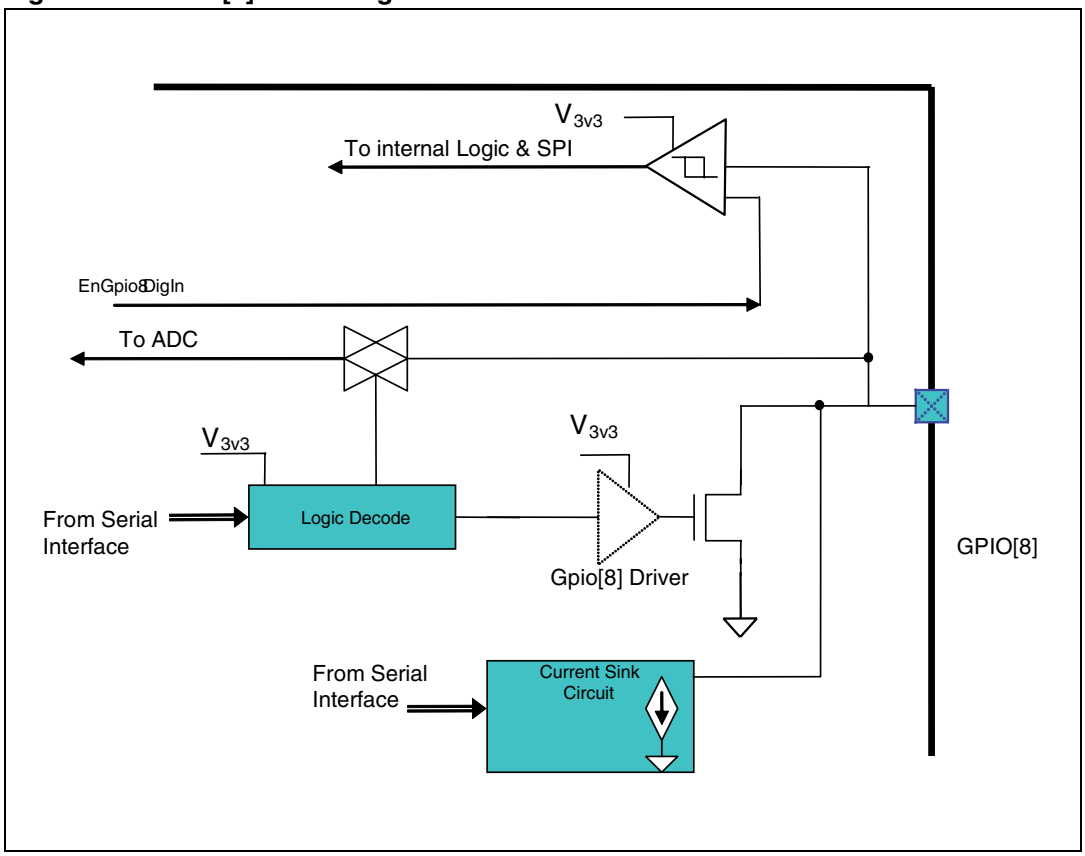


Table 86. GPIO[8] specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Input voltage hysteresis			0.22		V
V_{OL}	Low level output voltage	I_{OUT} = 15mA,			0.4	V
I_{LEAK_0}	Leakage current	EnGpio8DigIn=0, 0 ≤ Vout ≤ 5V	-1		1	µA
I_{LEAK_1}	Leakage current	EnGpio8DigIn=1, 0 ≤ Vout ≤ 5V	-1		5	µA
I_{AD}	A/D path absorbed current	ADChannelX[4:0] =10001 and bit EnDacScale=0	-1		1	µA
t_{DELAY}	Delay from serial write to pin low	C_{LOAD} =50 pF(1)			500	ns

1. Measured between nSS rising edge and 50% of V_{out}.

22.11 GPIO[9]

The GPIO[9] truth table is (for the abbreviation list please refer to *Table 68*):

Table 87. GPIO[9] truth

Op1EnPlusPin(1)	GPIO[9] SPI BITS				Function (2)	Note
	GpioOut enable[9]	Mode[2]	Mode[1]	Mode[0]		
1	X	X	X	X	OpAmp1 in+	(3)
0	0	X	X	X	HiZ (SPI_IN)	
0	1	0	0	0	SPI OUT	(4)
0	1	0	0	1	Interrupt Ctrl	(4)
0	1	0	1	0	AuxPwm2	(4)
0	1	0	1	1	Reg Loop 3	(4)
0	1	1	0	0	Interrupt Ctrl inverted	(4)
0	1	1	0	1	AuxPwm2 inverted	(4)
0	1	1	1	1	Reg Loop 3 inverted	(4)

1. The Op1EnPlusPin bit in the OpAmp1Ctrl register enables the connection of the positive input of Op1 to GPIO[9] pin.
2. The GPIO[9] pin is used by the system when firmware requires the ID read action (*Chapter 25*)
3. When Op1EnPlusPin = '1' the GpioOutEnable[9] bit is forced to 0.
4. In all configurations in which GPIO[9] is enabled as output:
   a) the GPIO[9] pin can be always used as an analog input to the ADC system (ADC function) by writing its address in the A2DChannelX[4:0] in the A2DConfigX register and starting a conversion;
   b) the GPIO[9] pin can be always used as a digital input so its value can be always read through SPI interface (SPI_IN function);
   c) please note that GPIO[9] output is directly connected to ExtPWM1 input for Bridge 1 or 2 and therefore particular care must be taken in order to avoid wrong PWM signals when ExtPWM1 is selected for bridge 1 or 2;
   d) the GPIO[9] pin is a rail to rail output supplied by V_{GPIO_SPI}.

Figure 37. GPIO[9] block diagram

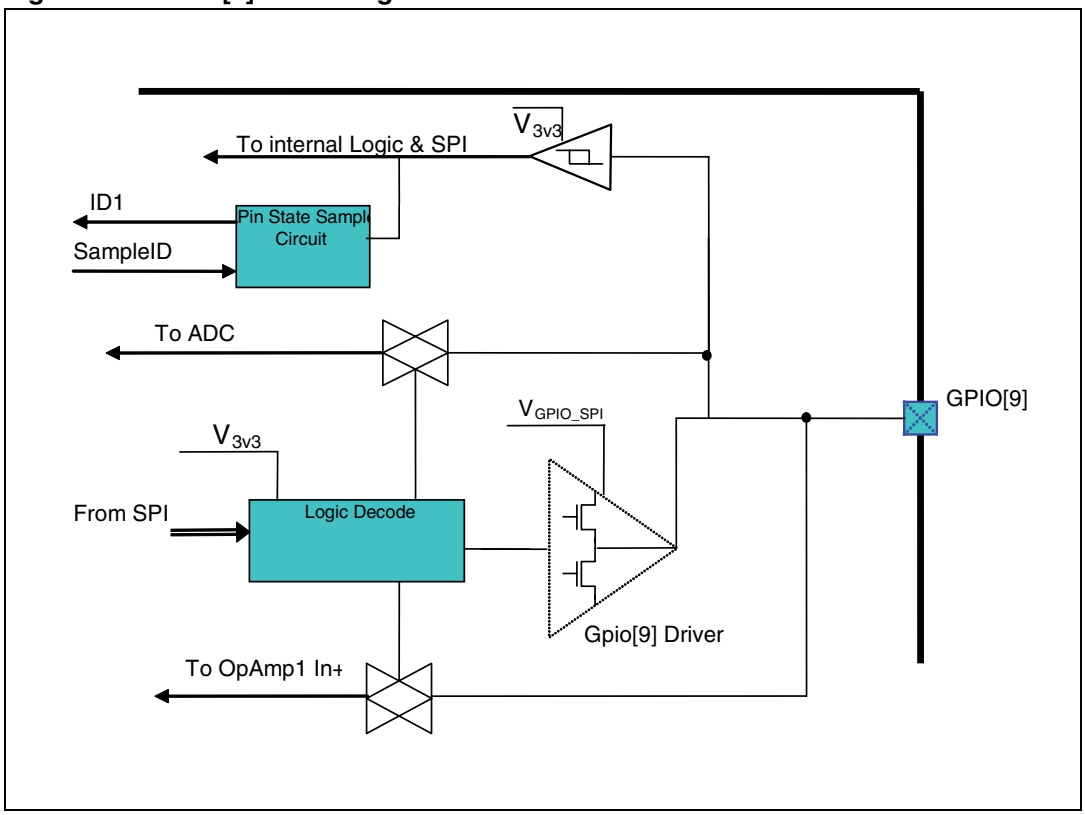


Table 88. GPIO[9] specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Input voltage hysteresis			0.22		V
V_{OL}	Low level output voltage	I_{OUT} = 15mA, V_{GPIO_SPI} = 3.15V			0.4	V
V_{OH}	High level output voltage	I_{OUT} = 15mA, V_{GPIO_SPI} = 3.15V	2.75			V
$I_{LEAKAGE}$	Leakage current	$0 \leq V_{out} \leq V_{GPIO\_SPI}$, V_{GPIO_SPI} = 3.15V	-1		1	µA
t_{DELAY}	Delay from serial write to pin low	C_{LOAD} =50 pF(1)			500	ns

1. Measured between nSS rising edge and 50% of V_{out}.

22.12 GPIO[10]

The GPIO[10] truth table is (for the abbreviation list please refer to *Table 68*):

Table 89. GPIO[10] truth

Op1EnPlusPin(1)	GPIO[10] SPI BITS				Function (2)	Note
	GpioOut enable[10]	Mode[2]	Mode[1]	Mode[0]		
1	X	X	X	X	OpAmp1 in-	(3)
0	0	X	X	X	HiZ (SPI_IN)	
0	1	0	0	0	SPI OUT	(4)
0	1	0	0	1	Interrupt Ctrl	(4)
0	1	0	1	0	AuxPwm2	(4)
0	1	0	1	1	AuxPwm3	(4)
0	1	1	0	0	Interrupt Ctrl inverted	(4)
0	1	1	0	1	AuxPwm2 inverted	(4)
0	1	0	0	0	AuxPwm3 inverted	(4)

1. The Op1EnMinusPin bit in the OpAmp1Ctrl register enables the connection of the positive input of Op1 to GPIO[10] pin.
2. The GPIO[10] pin is used by the system when firmware requires the ID read action (*Chapter 25*)
3. When Op1EnPlusPin = '1' the GpioOutEnable[10] bit is forced to 0.
4. In all configurations in which GPIO[10] is enabled as output:
   a) the GPIO[10] pin can be always used as an analog input to the ADC system (ADC function) by writing its address in the A2DChannelX[4:0] in the A2DConfigX register and starting a conversion;
   b) the GPIO[10] pin can be always used as a digital input so its value can be always read through SPI interface (SPI_IN function);
   c) please note that GPIO[10] output is directly connected to ExtPWM2 input for bridge 1 or 2 and therefore particular care must be taken in order to avoid wrong PWM signals when ExtPWM2 is selected for bridge 1 or 2;
   d) the GPIO[10] pin is a rail to rail output supplied by V_{GPIO_SPI}.

Figure 38. GPIO[10] block diagram

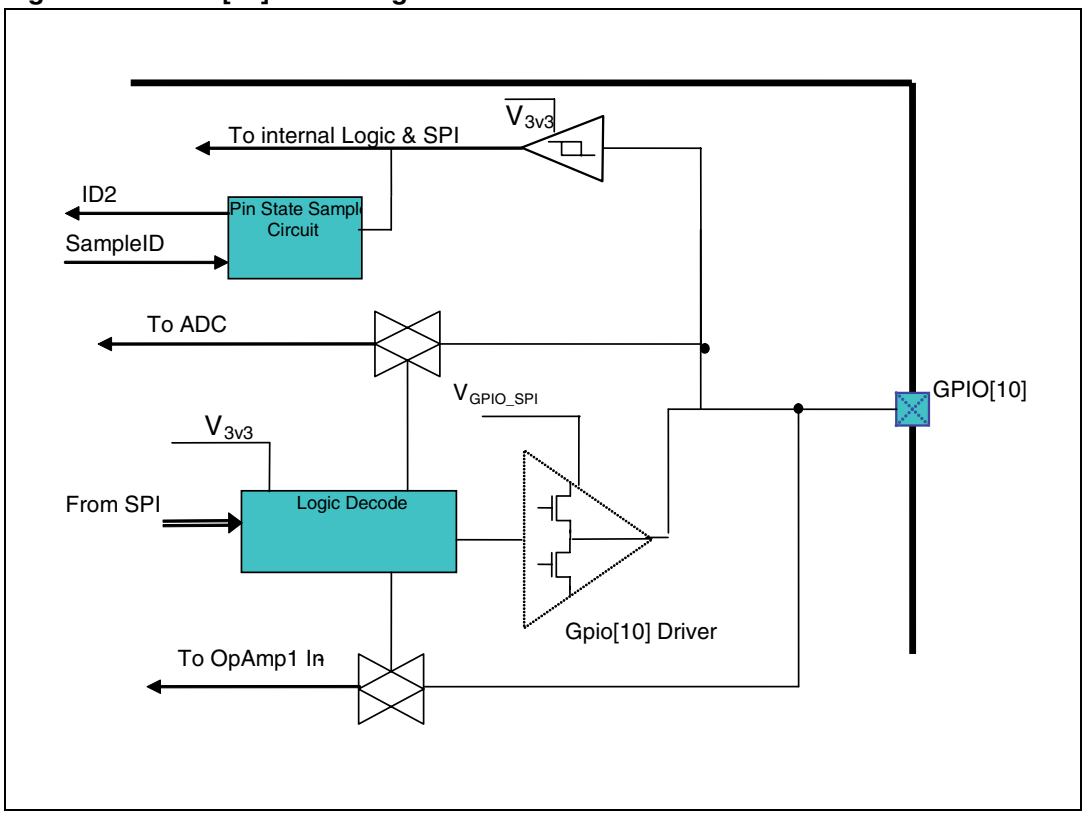


Table 90. GPIO[10] specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Input voltage hysteresis			0.22		V
V_{OL}	Low level output voltage	I_{OUT} = 15mA, V_{GPIO_SPI} = 3.15V			0.4	V
V_{OH}	High level output voltage	I_{OUT} = 15mA, V_{GPIO_SPI} = 3.15V	2.75			V
$I_{LEAKAGE}$	Leakage current	$0 \leq V_{out} \leq V_{GPIO\_SPI}$, V_{GPIO_SPI} = 3.15V	-1		1	µA
t_{DELAY}	Delay from serial write to pin low	C_{LOAD} =50 pF(1)			500	ns

1. Measured between nSS rising edge and 50% of V_{out}.

22.13 GPIO[11]

The GPIO[11] truth table is (for the abbreviation list please refer to *Table 68*):

Table 91. GPIO[11] truth

EnOpI (1)	GPIO[11] SPI BITS				Function	Note
	GpioOut enable[11]	Mode[2]	Mode[1]	Mode[0]		
1	X	X	X	X	OpAmp1 Out	(2)
0	0	X	X	X	HiZ (SPI_IN)	
0	1	0	0	0	SPI OUT	(3)
0	1	0	0	1	A2DGpo	(3)
0	1	0	1	0	AuxPwm1	(3)
0	1	0	1	1	AuxPwm2	(3)
0	1	1	0	0	SPI OUT inverted	(3)
0	1	1	0	1	A2DGpo inverted	(3)
0	1	1	1	0	AuxPwm1 inverted	(3)
0	1	1	1	1	AuxPwm2 inverted	(3)

1. The EnOp1 bit in the OpAmp1Ctrl register enables the operational amplifier 1.
2. When EnOp1 = '1' the GpioOutEnable[11] bit is forced to 0.
3. In all configurations in which GPIO[11] is enabled as output:
   a) the GPIO[11] pin can be always used as an analog input to the ADC system (ADC function) by writing its address in the A2DChannelX[4:0] in the A2DConfigX register and starting a conversion;
   b) the GPIO[11] pin can be always used as a digital input so its value can be always read through SPI interface (SPI_IN function);
   c) please note that GPIO[11] output is directly connected to ExtPWM4 input for bridge 3 or 4 and therefore particular care must be taken in order to avoid wrong PWM signals when ExtPWM4 is selected for bridge 3 or 4;
   d) the GPIO[11] pin is a rail to rail output supplied by V_{GPIO_SPI}.

Figure 39. GPIO[11] block diagram

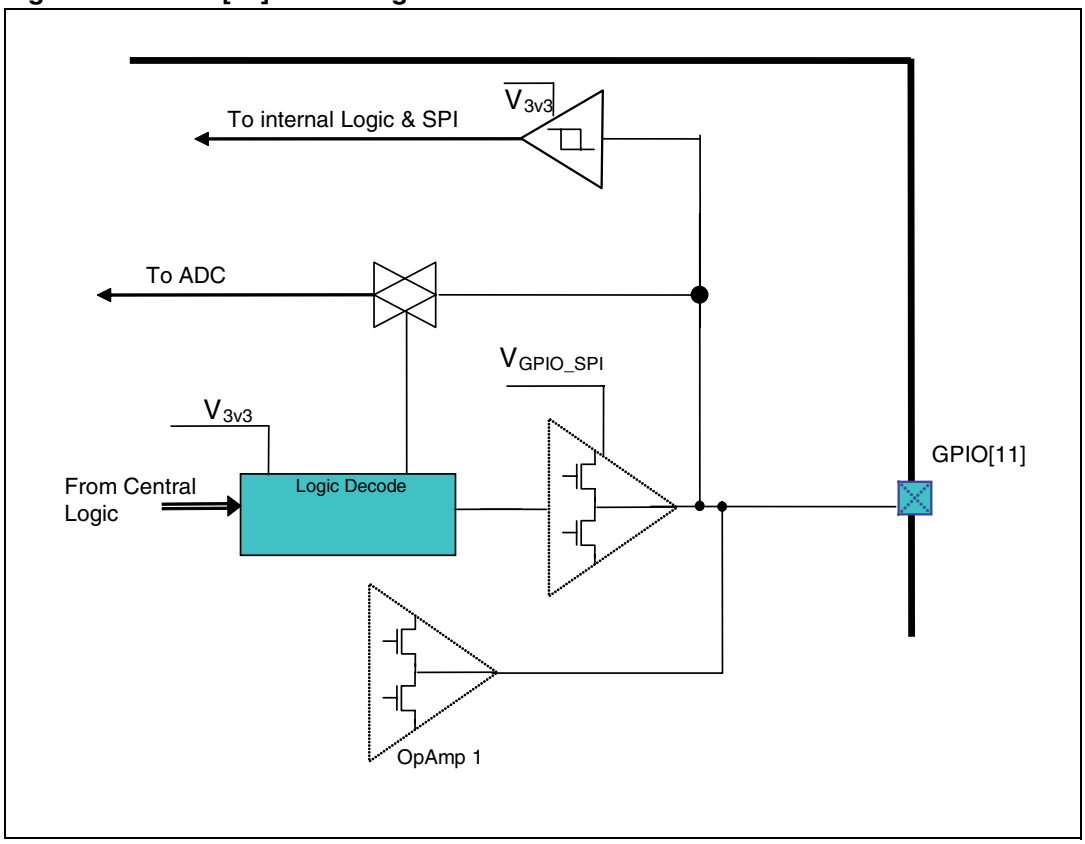


Table 92. GPIO[11] specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Input voltage hysteresis			0.22		V
V_{OL}	Low level output voltage	I_{OUT} = 15mA, V_{GPIO_SPI} = 3.15V			0.4	V
V_{OH}	High level Output voltage	I_{OUT} = -15mA, V_{GPIO_SPI} = 3.15V	2.75			V
$I_{LEAKAGE}$	Leakage current	$0 \leq V_{out} \leq V_{GPIO\_SPI}$, V_{GPIO_SPI} = 3.15V	-1		1	µA
t_{DELAY}	Delay from serial write to pin low	C_{LOAD} =50 pF(1)			500	ns

1. Measured between nSS rising edge and 50% of V_{out}.

22.14 GPIO[12]

The GPIO[12] truth table is (for the abbreviation list please refer to *Table 68*):

Table 93. GPIO[12] truth

AUX2enable or AUX2system (1)	Op2En PlusPin	GPIO[12] SPI BITS				Function	Note
		GpioOut enable[12]	Mode[2]	Mode[1]	Mode[0]		
1	X	X	X	X	X	RegLoop2	
0	1	X	X	X	X	OpAmp2 in+	(2)
0	0	0	X	X	X	HiZ (SPI_IN)	
0	0	1	0	0	0	SPI OUT	(3)
0	0	1	0	0	1	Interrupt Ctrl	(3)
0	0	1	0	1	0	Comp2OUT	(3)
0	0	1	0	1	1	RegLoop2	(3)
0	0	1	1	0	0	Interrupt Ctrl inverted	(3)
0	0	1	1	0	1	Comp2OUT inverted	(3)
0	0	1	1	1	1	RegLoop2 inverted	(3)

1. AUX2Enable or AUX2System bit =1 represent the case in which AUX2 is used as a regulator (system or not system).
2. When Op2EnPlusPin = '1' the GpioOutEnable[11] bit is forced to 0.
3. In all configurations in which GPIO[12] is enabled as output:
   a) the GPIO[12] pin can be always used as an analog input to the ADC system (ADC function) by writing its address in the A2DChannelX[4:0] in the A2DConfigX register and starting a conversion;
   b) the GPIO[12] pin can be always used as a digital input so its value can be always read through SPI interface (SPI_IN function);
   c) please note that GPIO[12] output is directly connected to StepCmd input for stepper driver and therefore particular care must be taken in order to avoid wrong PWM signals when StepCmd is selected for stepper driver (STEP_REQUEST function)
   d) the GPIO[12] pin is a rail to rail, back to back output supplied by V_{GPIO_SPI}.

Figure 40. GPIO[12] block diagram

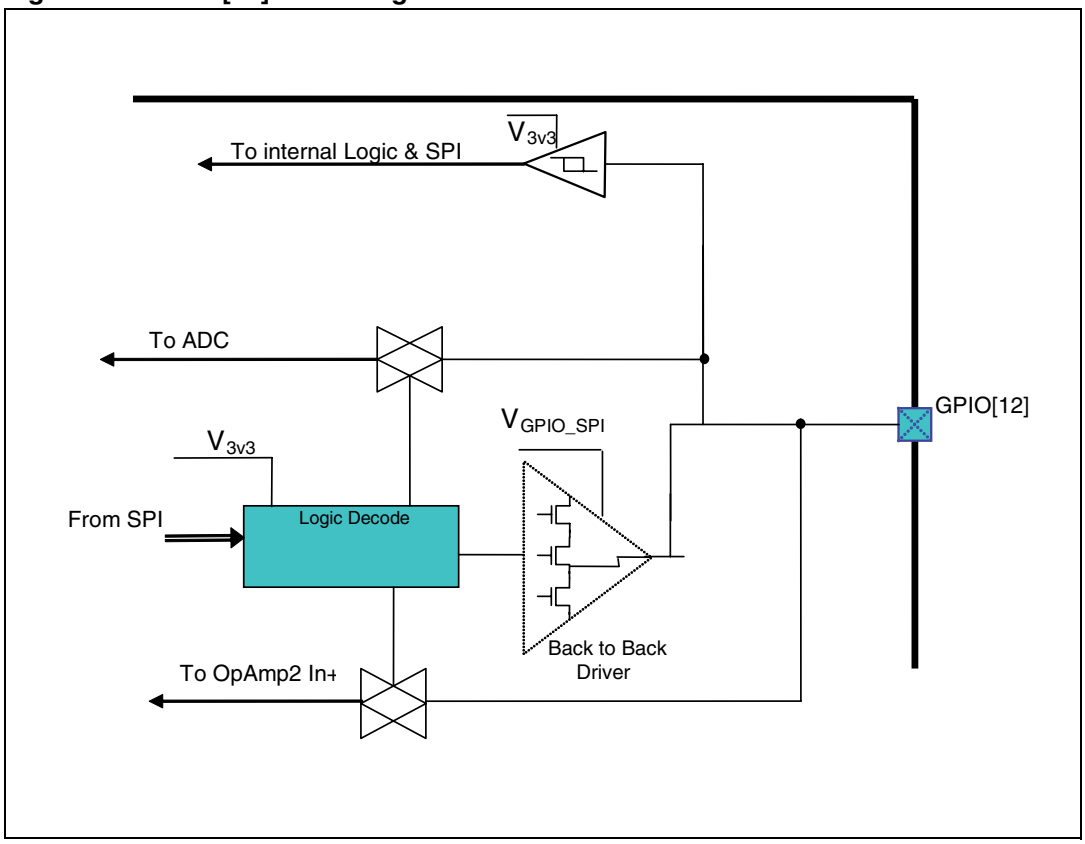


Table 94. GPIO[12] specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Input voltage hysteresis			0.22		V
V_{OL}	Low level output voltage	I_{OUT} = 15mA, V_{GPIO_SPI} = 3.15V			0.4	V
V_{OH}	High level output voltage	I_{OUT} = 15mA, V_{GPIO_SPI} = 3.15V	2.75			V
$I_{LEAKAGE}$	Leakage current	$0 \leq V_{out} \leq V_{GPIO\_SPI}$, V_{GPIO_SPI} = 3.15V	-1		1	µA
t_{DELAY}	Delay from Serial Write to pin Low	C_{LOAD} =50 pF (1)			500	ns

1. Measured between nSS rising edge and 50% of V_{out}.

22.15 GPIO[13]

The GPIO[13] truth table is (for the abbreviation list please refer to *Table 68*):

Table 95. GPIO[13] truth

Op2En mimusPin(1)	GPIO[13] SPI BITS				Function	Note
	GpioOut enable[13]	Mode[2]	Mode[1]	Mode[0]		
1	X	X	X	X	OpAmp2 in-	(2)
0	0	X	X	X	HiZ (SPI_IN)	
0	1	0	0	0	SPI OUT	(3)
0	1	0	0	1	AuxPwm1	(3)
0	1	0	1	0	Reg Loop 3	(3)
0	1	0	1	1	AuxPwm3	(3)
0	1	1	0	0	AuxPwm1 inverted	(3)
0	1	1	0	1	Reg Loop 3 inverted	(3)
0	1	1	1	1	AuxPwm3 inverted	(3)

1. The Op2EnMinusPin bit in the OpAmp2Ctrl register enables the connection of the positive input of Op1 to GPIO[13] pin.
2. When Op2EnMinusPin = '1' the GpioOutEnable[13] bit is forced to 0.
3. In all configurations in which GPIO[9] is enabled as output:
   a) the GPIO[13] pin can be always used as an analog input to the ADC system (ADC function) by writing its address in the A2DChannelX[4:0] in the A2DConfigX register and starting a conversion;
   b) the GPIO[13] pin can be always used as a digital input so its value can be always read through SPI interface (SPI_IN function);
   c) the GPIO[13] pin is a rail to rail output supplied by V_{GPIO_SPI}.

Figure 41. GPIO[13] block diagram

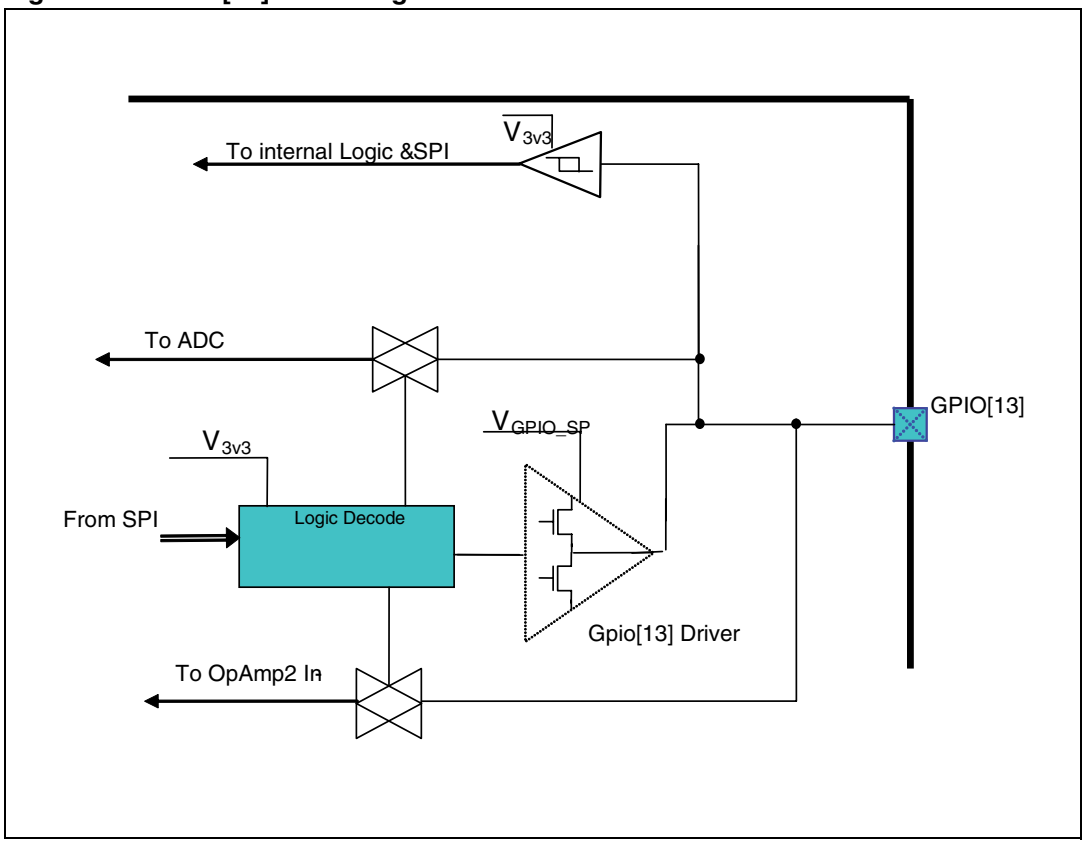


Table 96. GPIO[13] specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Input voltage hysteresis			0.22		V
V_{OL}	Low level output voltage	I_{OUT} = 15mA, V_{GPIO_SPI} = 3.15V			0.4	V
V_{OH}	High level output voltage	I_{OUT} = 15mA, V_{GPIO_SPI} = 3.15V	2.75			V
$I_{LEAKAGE}$	Leakage current	$0 \le V_{out} \le V_{GPIO\_SPI}$, V_{GPIO_SPI} = 3.15V	-1		1	µA
t_{DELAY}	Delay from serial write to pin low	C_{LOAD} =50 pF(1)			500	ns

1. Measured between nSS rising edge and 50% of V_{out}.

22.16 GPIO[14]

The GPIO[14] truth table is (for the abbreviation list please refer to *Table 68*):

Table 97. GPIO[14] truth

EnOp2[1]	GPIO[14] SPI BITS				Function	Note
	GpioOut enable[14]	Mode[2]	Mode[1]	Mode[0]		
1	X	X	X	X	OpAmp2 Out	(2)
0	0	X	X	X	HiZ (SPI_IN)	
0	1	0	0	0	SPI OUT	(3)
0	1	0	0	1	Interrupt Ctrl	(3)
0	1	0	1	0	AuxPwm2	(3)
0	1	0	1	1	AuxPwm3	(3)
0	1	1	0	0	SPI OUT inverted	(3)
0	1	1	0	1	Interrupt Ctrl inverted	(3)
0	1	1	1	0	AuxPwm2 inverted	(3)
0	1	1	1	1	AuxPwm3 inverted	(3)

1. The EnOp2 bit in the OpAmp2Ctrl register enables the operational amplifier 2.
2. When EnOp2 = '1' the GpioOutEnable[14] bit is forced to 0.
3. In all configurations in which GPIO[14] is enabled as output:
   a) the GPIO[14] pin can be always used as an analog input to the ADC system (ADC function) by writing its address in the A2DChannelX[4:0] in the A2DConfigX register and starting a conversion;
   b) the GPIO[14] pin can be always used as a digital input so its value can be always read through SPI interface (SPI_IN function);
   c) the GPIO[14] pin is a rail to rail output supplied by V_{GPIO_SPI}.

Figure 42. GPIO[14] block diagram

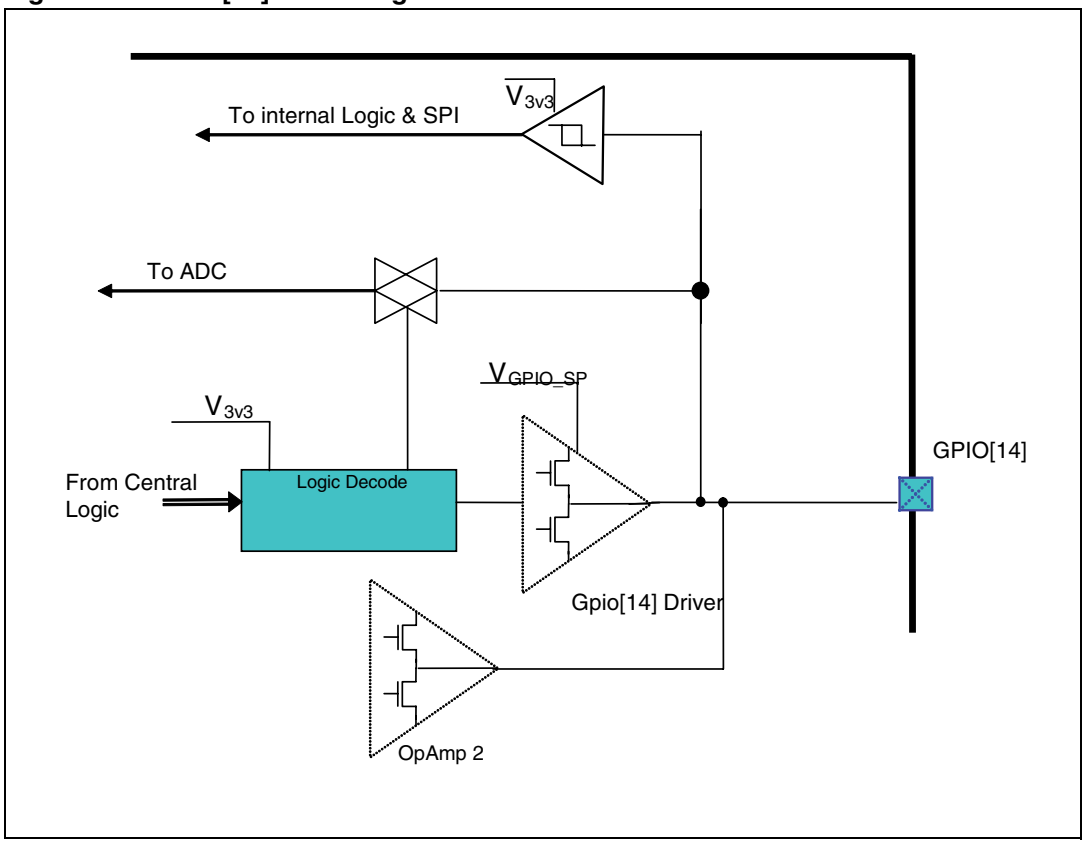


Table 98. GPIO[14] specification

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.8	V
V_{HYS}	Input voltage hysteresis			0.22		V
V_{OL}	Low level output voltage	I_{OUT} = 15mA, V_{GPIO_SPI} = 3.15V			0.4	V
V_{OH}	High level output voltage	I_{OUT} = 15mA, V_{GPIO_SPI} = 3.15V	2.75			V
$I_{LEAKAGE}$	Leakage current	$0 \leq V_{out} \leq V_{GPIO\_SPI}$, V_{GPIO_SPI} = 3.15V	-1		1	µA
t_{DELAY}	Delay from serial write to pin low	C_{LOAD} =50 pF(1)			500	ns

1. Measured between nSS rising edge and 50% of V_{out}.

23 Serial interface

S.A.B.Re can communicate with an external microprocessor by using an integrated slave SPI (Serial Protocol Interface). Through this interface almost all S.A.B.Re functionalities can be controlled and all the ICs can be seen as a register map made by 128 register of 16-bit each.

The SPI is a simple industry standard communications interface commonly used in embedded systems and it has the following four I/O pins:

- Miso (master input slave output)
- Mosi (Master Output Slave Input)
- sclk (serial clock [controlled by the master])
- nSS (slave select active low [controlled by the master])

The “Miso” (master in, slave out) signal carries synchronous data from the slave to the master device. The mosi (master out, slave in) signal carries synchronous data from the master to the slave device. The sclk signal is driven by the master, synchronizing all data transfers. Each SPI slave device has one nSS signal that is an active-low slave input/master output pin. Slave devices do not respond to transactions unless their nSS input signal is driven low. Master device interfacing with multiple SPI slave devices has an nSS signal for each slave device.

S.A.B.Re will maintain its miso pin in high impedance until it does not recognize its address in serial frame.

23.1 Read transaction

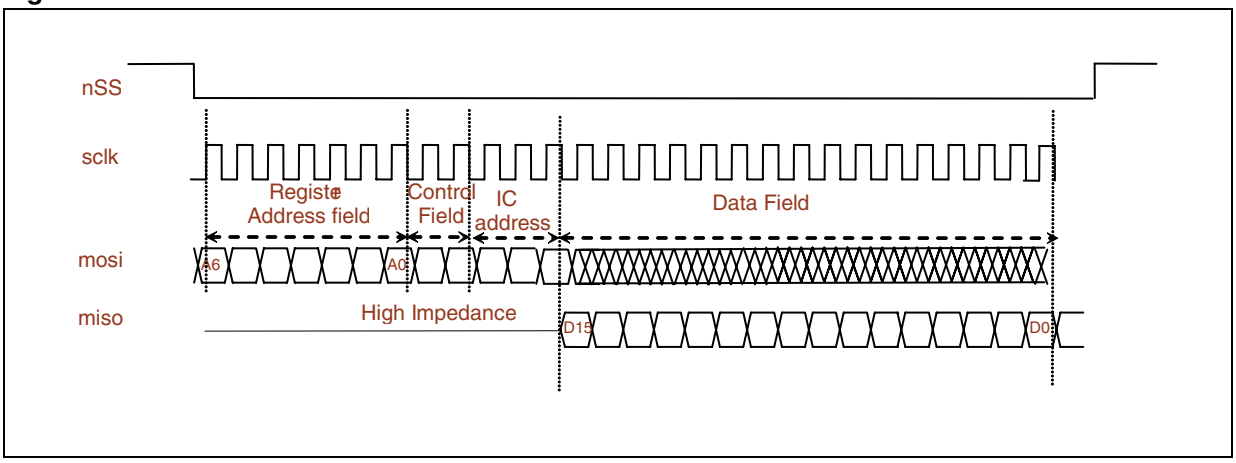
A read transaction (see *Figure 43*) is always started by the master device that lowers the nSS pin. The other bits are then sent on the mosi pin with this order:

1. 7-bit representing the address of the register that must be read (MSB first [A_6…A_0]);
2. 2-bit that must be “10” for a read transaction;
3. 2-bit representing S.A.B.Re IC address;
4. 1-bit reserved for future use that must be set at “0”.

At this point the data stored in the register at the selected address will be shifted out on the miso pin.

The read operation is terminated by raising the signal on nSS pin.

Figure 43. SPI read transaction



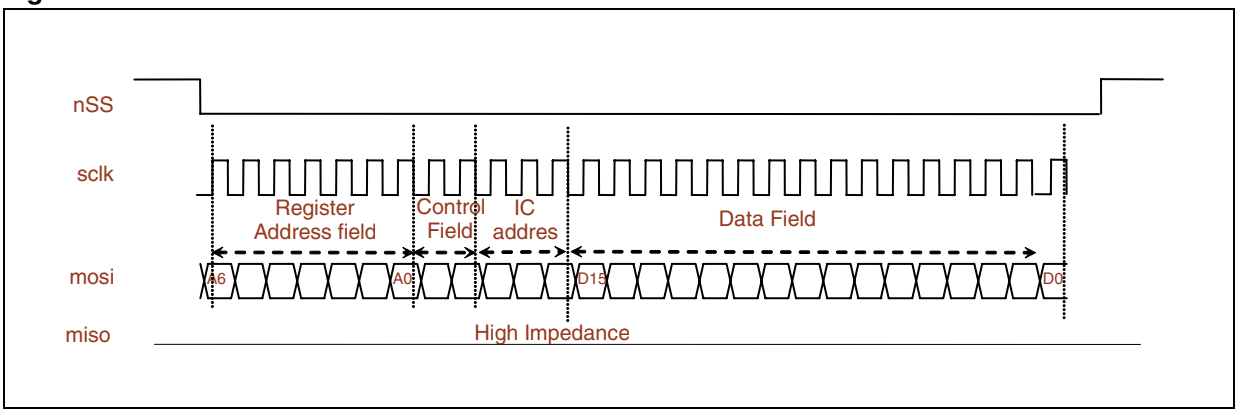
23.2 Write transaction

A write transaction (see *Figure 44*) is always started by the master lowering the signal on nSS pin. The other bits are then sent on the mosi pin with this order:

1. 7-bit representing the address of the register that must be written (MSB first [A6…A0]);
2. 2-bit that must be “01” for a read transaction;
3. 2-bit representing S.A.B.Re IC address;
4. 1-bit reserved for future use that must be set at “0”.

The data to be written (MSB first D15…D0) are then read from mosi pin. The length of data field can be 16 or 20 bits, but only the first 16-bit are accepted as valid data. Data is latched on rising edge of the nSS line.

Figure 44. SPI write transaction



The SPI input and output timing definitions are shown in the following tables:

Figure 45. SPI input timing diagram

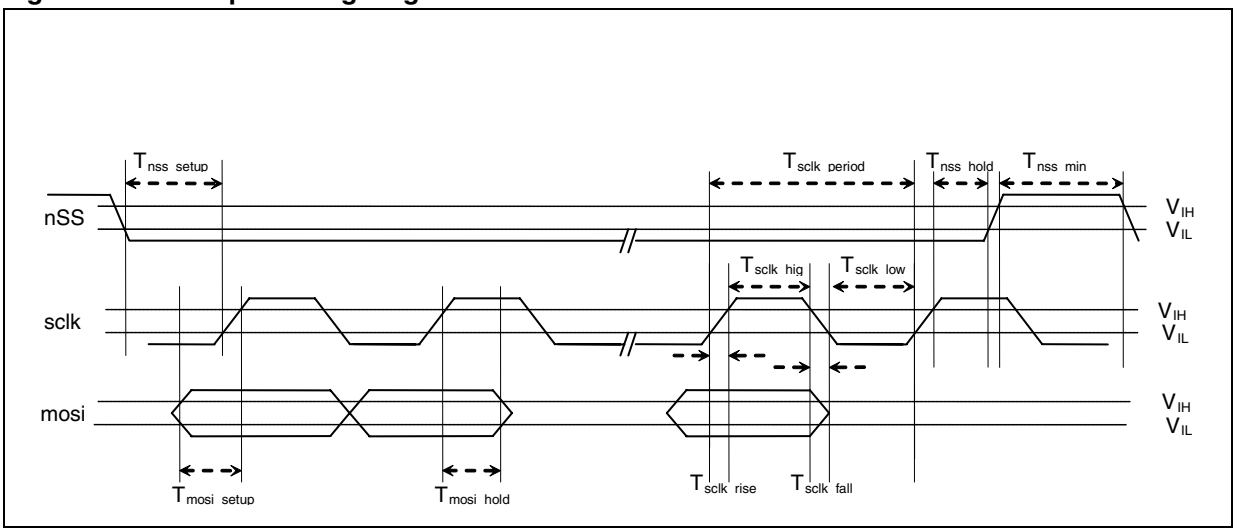


Figure 46. SPI output timing diagram

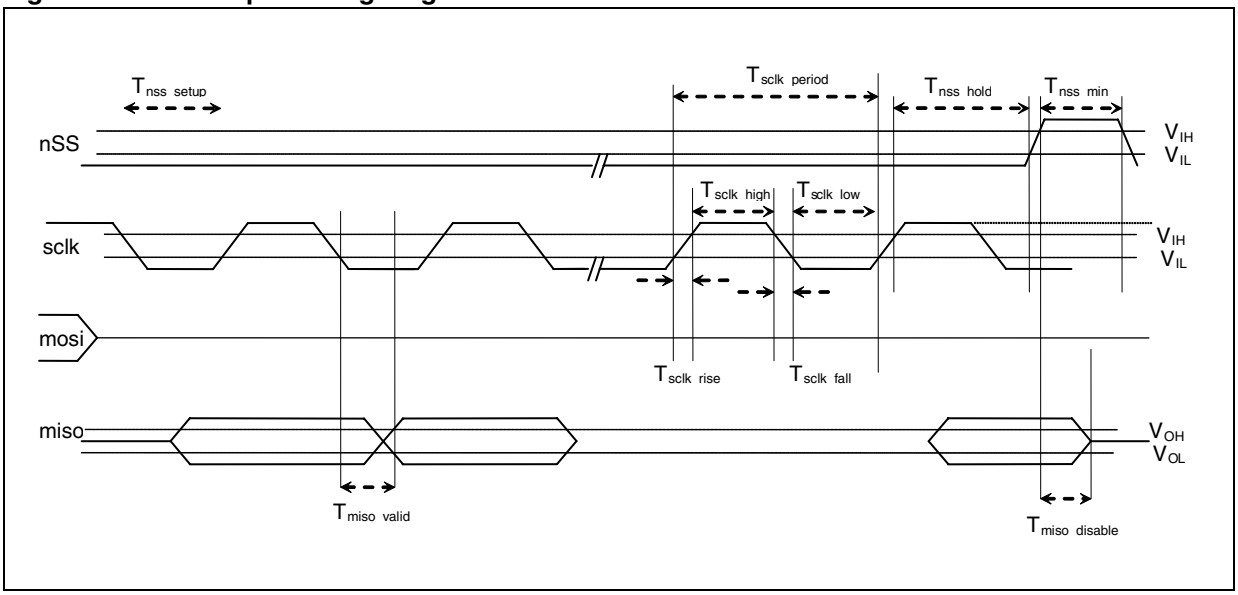


Table 99. SPI interface specifications

(Note: V_{GPIO_SPI}=3.3V unless otherwise specified)

Parameter	Description	Test condition	Min	Typ	Max	Unit
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage	(1)			0.8	V
V_{HYS}	Input voltage hysteresis	(1)		0.22		V
V_{OH}	High level output voltage	I_{OUT} = -10mA,(2)	2.75			V
V_{OL}	Low level output voltage	I_{OUT} = 10mA,(2)			0.4	V
t_{sclk_period}	SCLK period		62.5			ns
t_{sclk_rise}	SCLK rise time				2	ns
t_{sclk_fall}	SCLK fall time				2	ns
t_{sclk_high}	SCLK high time		20			ns
t_{sclk_low}	SCLK low time		20			ns
t_{nss_setup}	nSS setup time		10			ns
t_{nss_hold}	nSS hold time		10			ns
t_{nss_min}	nSS high minimum time		30			ns
t_{mosi_setup}	Mosi setup time		10			ns
t_{mosi_hold}	Mosi hold time		10			ns
t_{miso_rise}	Miso rise time	C_{LOAD}=50pF(3)			9	ns
t_{miso_fall}	Miso fall time	C_{LOAD}=50pF (3)			9	ns
t_{miso_valid}	Miso valid from clock low		0		15	ns
$t_{miso\_disable}$	Miso disable time		0		15	ns
C_{LOAD}	Miso maximum load				200	pF

1. Specification applies to nSS, sclk and mosi pins.
2. Current is considered to be positive when flowing towards the IC
3. These times are measured at the pin output between specified V_{OH} and V_{OL}.

24 Registers list

Many of the S.A.B.Re functionalities are controlled or can be supervised by accessing to the relative register through serial interface. All these registers can be seen from the user (microcontroller) point of view as a register table. Each register is one word wide (16-bit) and can be read using a 7-bit address

Table 100. Register address map

Address[6:0] (binary)	Name	Comment	Address[6:0] (binary)	Name	Comment
000_0000	DevName	Read only	100_0000	AuxPwm1Ctrl	
000_0001	CoreConfigReg		100_0001	AuxPwm2Ctrl	
000_0010	ICTemp		100_0010	GpPwm3Base	
000_0011	ICStatus		100_0011	GpPwm3Ctrl	
000_0100	EnTestRegs		100_0100		
000_0101	SampleID		100_0101		
000_0110	WatchDogCfg		100_0110	IntCtrlCfg	
000_0111	WatchDogStatus		100_0111	IntCtrlCtrl	
000_1000	SoftResReg		100_1000	DigCmpCfg	
000_1001			100_1001	DigCmpValue	
000_1010			100_1010		
000_1011			100_1011		
000_1100	HibernateStatus		100_1100		
000_1101	HibernateCmd		100_1101		
000_1110			100_1110		
000_1111	Mtr1_2PwrCtrl		100_1111		
001_0000	MainVSwCfg		101_0000	A2DControl	
001_0001			101_0001	A2DConfig1	
001_0010	MainlinCfg		101_0010	A2DResult1	
001_0011			101_0011	A2DConfig2	
001_0100	SwCtrCfg		101_0100	A2DResult2	
001_0101			101_0101		
001_0110			101_0110		
001_0111			101_0111		
001_1000	StdByMode		101_1000	GpioOutEnable	
001_1001			101_1001	GpioCtrl1	
001_1010			101_1010	GpioCtrl2	
001_1011			101_1011	GpioCtrl3	

Table 100. Register address map (continued)

Address[6:0] (binary)	Name	Comment	Address[6:0] (binary)	Name	Comment
001_1100			101_1100	GpioPadVal	Read only
001_1101			101_1101	GpioOutVal	
001_1110			101_1110		
001_1111			101_1111		
010_0000	Mtrs1_2Cfg		110_0000	LowVSwitchCtrl	
010_0001	Mtr1Cfg		110_0001		
010_0010	Mtr1Ctrl		110_0010		
010_0011	Mtr1Limit		110_0011		
010_0100	Mtr2Cfg		110_0100	OpAmpCtrl1	
010_0101	Mtr2Ctrl		110_0101	OpAmpCtrl2	
010_0110	Mtr2Limit		110_0110		
010_0111			110_0111		
010_1000	Mtrs3_4Cfg		110_1000		
010_1001	Mtr3Cfg		110_1001		
010_1010	Mtr3Ctrl		110_1010		
010_1011	Mtr3ILimit		110_1011		
010_1100	Mtr4Cfg		110_1100		
010_1101	Mtr4Ctrl		110_1101		
010_1110	Mtr4ILimit		110_1110		
010_1111			110_1111		
011_0000	StpCfg1		111_0000		
011_0001	StpCfg2		111_0001		
011_0010	StpCtrl		111_0010		
011_0011	StpCmd		111_0011		
011_0100	StpTest		111_0100		
011_0101	Aux1SwCfg		111_0101		
011_0110	Aux2SwCfg		111_0110		
011_0111	Aux3SwCfg1		111_0111		
011_1000	Aux3SwCfg2		111_1000		
011_1001	Power Mode Control		111_1001		
011_1010			111_1010		
011_1011			111_1011	REV_MFCT	
011_1100	CurrDacCtrl		111_1100	RESERVED	

Table 100. Register address map (continued)

Address[6:0] (binary)	Name	Comment	Address[6:0] (binary)	Name	Comment
011_1101			111_1101	RESERVED	
011_1110			111_1110	RESERVED	
011_1111			111_1111	RESERVED	

25 Schematic samples

Figure 47. Application with 2 DC motors, 1 stepper motor and 3 power supplies

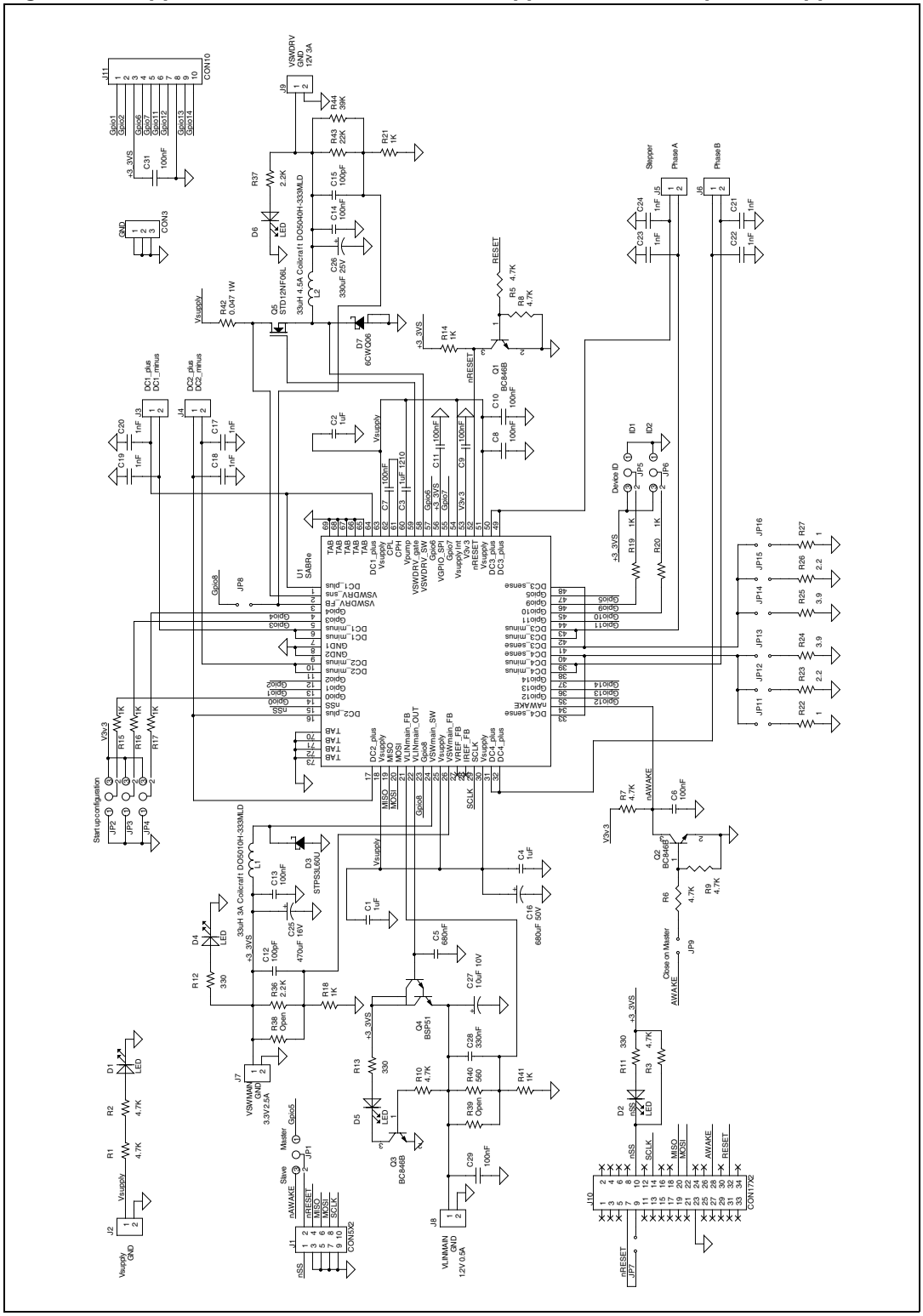
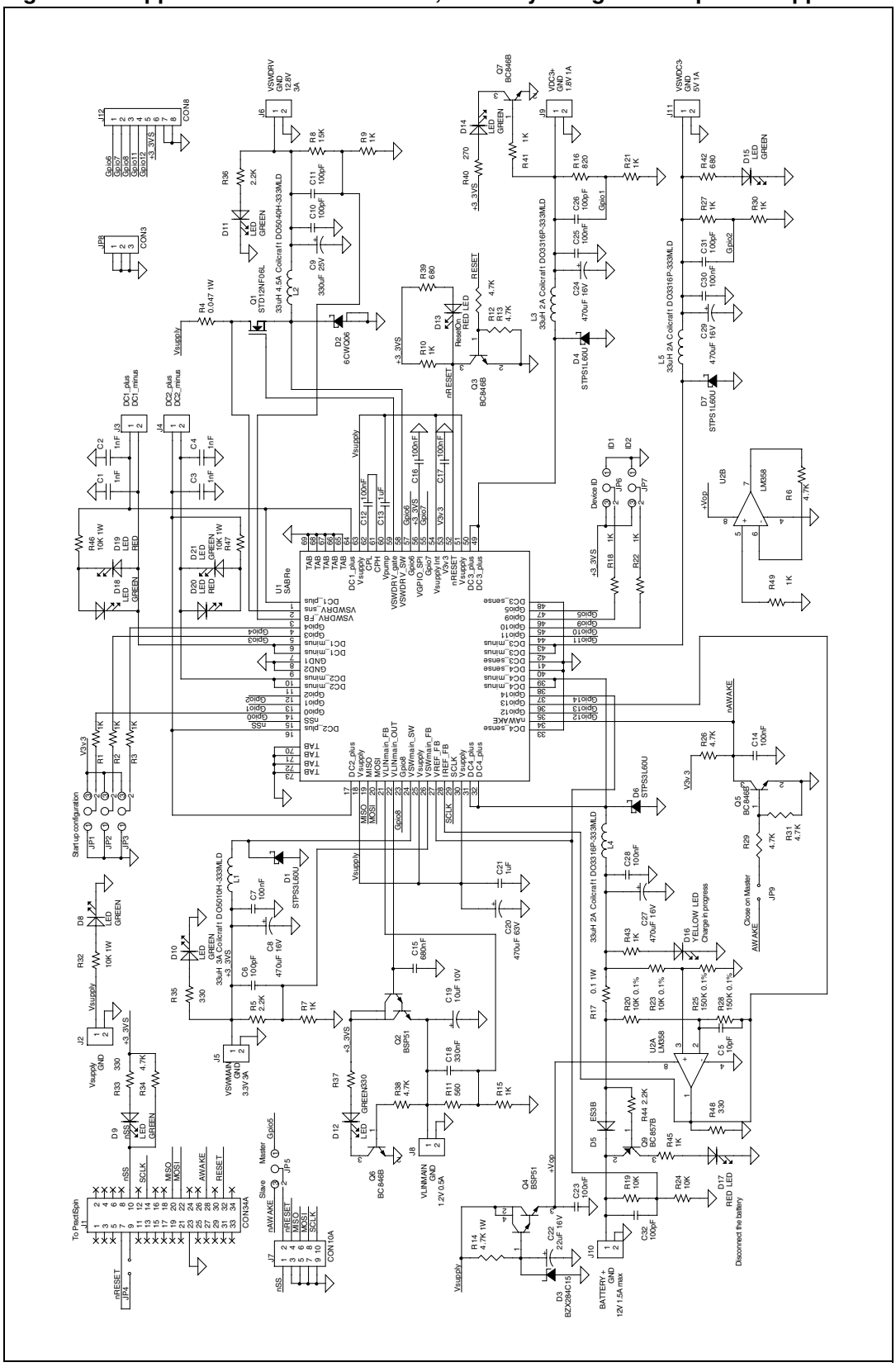


Figure 48. Application with 2 DC motors, a battery charger and 5 power supplies



26 Pin list

26.1 Pin list

Table 101. Pins configuration

Pin #	Pin name	Description	Type
1	DC1_PLUS	Bridge 1 phase “plus” output	Output
2	V_{SWDRV_SNS}	Switching regulator controller sense	Analog input
3	V_{SWDRV_FB}	Switching regulator controller feedback	Analog input
4	GPIO4	General purpose I/O	Analog In/Out - CMOS bi-dir
5	GPIO3	General purpose I/O	Analog In/Out - CMOS bi-dir
6	DC1_MINUS	Bridge 1 phase “minus” output	Output
7	DC1_MINUS	Bridge 1 phase “minus” output	Output
8	GND1	Ground pin for bridge1 (1)(2)(3)	Power/digital
9	GND2	Ground pin for bridge2 (1)(2)(3)	Power/digital
10	DC2_MINUS	Bridge 2 phase “minus” output	Output
11	DC2_MINUS	Bridge 2 phase “minus” output	Output
12	GPIO2	General purpose I/O	Analog In/Out - CMOS bi-dir
13	GPIO1	General purpose I/O	Analog In/Out - CMOS bi-dir
14	GPIO0	General purpose I/O	Analog Input - CMOS input
15	nSS	SPI chip select pin	CMOS input
16	DC2_PLUS	Bridge 2 phase “plus” output	Output
17	DC2_PLUS	Bridge 2 phase “plus” output	Output
18	V_{Supply}	Main voltage supply	Power input
19	MISO	SPI serial data output	CMOS output
20	MOSI	SPI serial data input	CMOS input
21	$V_{LINmain\_FB}$	Linear main regulator feedback	Analog input
22	$V_{LINmain\_OUT}$	Linear main regulator output	Power output
23	GPIO 8	General purpose I/O	Analog In/Out - CMOS bi-dir
24	V_{SWmain_SW}	Main switching regulator switching output	Power output
25	V_{Supply}	Main voltage supply	Power Input
26	V_{SWmain_FB}	Main switching regulator feedback pin	Analog input
27	V_{REF_FB}	Regulator voltage feedback	Analog input
28	I_{REF_FB}	Regulator current feedback	Analog input
29	SCLK	SPI input clock pin	CMOS input
30	V_{Supply}	Main voltage supply	Power input
31	DC4_PLUS	Bridge 4 phase “plus” output	Output

Table 101. Pins configuration (continued)

Pin #	Pin name	Description	Type
32	N.C.	Not connected	
33	DC4_SENSE	Bridge 4 sense output(4)	Output
34	nAWAKE	Device wake up	CMOS input
35	GPIO12	General purpose I/O	Analog In/Out - CMOS bi-dir
36	GPIO13	General purpose I/O	Analog In/Out - CMOS bi-dir
37	GPIO14	General purpose I/O	Analog In/Out - CMOS bi-dir
38	N.C.	Not connected	
39	DC4_MINUS	Bridge 4 phase “minus” output	Output
40	DC4_SENSE	Bridge 4 sense output(4)	Output
41	DC3_SENSE	Bridge 3 sense output(4)	Output
42	DC3_MINUS	Bridge 3 phase “minus” output	Output
43	N.C.	Not connected	
44	GPIO11	General purpose I/O	Analog In/Out - CMOS bi-dir
45	GPIO10	General purpose I/O	Analog In/Out - CMOS bi-dir
46	GPIO9	General purpose I/O	Analog In/Out - CMOS bi-dir
47	GPIO5	General purpose I/O	Analog In/Out - CMOS bi-dir
48	DC3_SENSE	Bridge 3 sense output(4)	Output
49	N.C.	Not connected	
50	DC3_PLUS	Bridge 3 phase “plus” output	Output
51	V_{Supply}	Main voltage supply	Power input
52	nRESET	Open drain system reset pin	CMOS Input/output
53	V_{3v3}	Internal 3.3 volt regulator	Power Input/output
54	$V_{SupplyInt}$	Internal voltage supply	Power Input
55	GPIO7	General purpose I/O	Analog In/Out - CMOS bi-dir
56	V_{GPIO_SPI}	Low voltage pins power supply	Power input
57	GPIO6	General purpose I/O	Analog In/Out - CMOS bi-dir
58	V_{SWDRV_SW}	Switching regulator controller source input	Power input
59	V_{SWDRV_GATE}	Switching driver gate drive pin	Analog output
60	V_{Pump}	Charge pump voltage	Power Input/output
61	CPH	Charge pump high switch pin	Power Input/output
62	CPL	Charge pump low switch pin	Power Input/output
63	V_{Supply}	Main voltage supply	Power input
64	DC1_plus	Bridge 1 phase “plus” output	Output
E_Pad	GND_PAD	(1)(2)(3)	

1. These pins must be connected all together to a unique PCB ground.
2. Bridges1 and 2 have 2 ground pads: one is bonded to the relative ground pin (GND1 or GND2) and the other is connected to exposed pad (E_Pad) ground ring. This makes the bond wires testing possible by forcing a current between E-Pad and GND1 or GND2 pins and using the other pin as sense pin to measure the resistance of E-Pad bonding. (N.B: grounds of two bridges are internally connected together).
3. The analog ground is connected to exposed pad E-Pad.
4. The pin must be tied to ground if bridge is not used as a stepper motor.

27 Package information

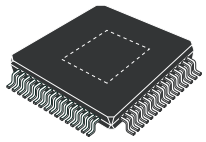
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

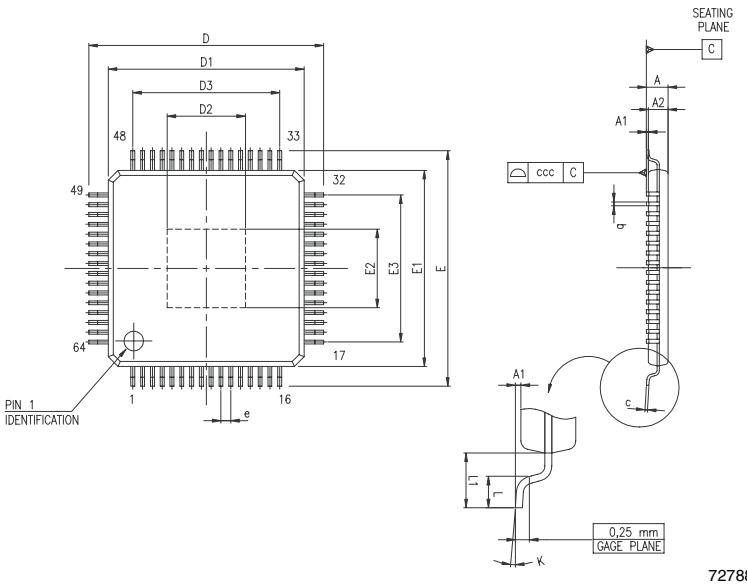
Figure 49. TQFP64 mechanical data & package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.20			0.0472
A1	0.05		0.15	0.002		0.006
A2	0.95	1.00	1.05	0.0374	0.0393	0.0413
b	0.17	0.22	0.27	0.0066	0.0086	0.0086
c	0.09		0.20	0.0035		0.0078
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D2	2.00			0.787		
D3		7.50			0.295	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E2	2.00			0.787		
E3		7.50			0.295	
e		0.50			0.0197	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
k	0°	3.5°	7°	0°	3.5°	7°
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



TQFP64 (10x10x1.0mm) Exposed Pad Down



28 Revision history

Table 102. Document revision history

Date	Revision	Changes
14-Nov-2007	1	Initial release.

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